TYPE 547 NOTES

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by J. Power

Written and Produced in Field Training

Chuck Miller

TYPE 547 INTRODUCTION

GENERAL DESCRIPTION

A. General Purpose Laboratory Scope

1. Basically a Type 546 with alternate sweep switching added.
2. Vertical is compatible with letter series plug-ins.
3. Rackmount available.

B. Vertical

1. Designed for "1" series plug-ins, but will accept letter series.
2. Passband of 50 mc with Type 1A1.
   a. Risetime with 1A1 is 6.25 nsec.
3. Completely transistorized so no thermal drift problem.
4. Fixed-tuned delay line.
5. VERTICAL SIG OUT jack on the front panel.
   a. AC coupled at .35 v/cm.

C. Horizontal

1. Identical A and B sweeps.
   a. Sweep rates 5 sec to .1 μsec unmagnified.
   b. X1, X2, X5, X10 MAG.
   c. No stability control.
   d. Sweep will free-run in absence of triggers when TRIGGERING control is switched to AUTO. ("Bright line automatic")

2. Horizontal Display Switch.

   a. A, B, A ALT B.

   b. B INTEN BY A, A DLY'D BY B, or Alternate.

   c. External Horizontal, X1, X10.

3. Alternate.

   a. A Sweep or B Sweep displayed alternately.

   b. Trace separation shifts VERTICAL so both traces can be observed -- amount of separation controlled by front panel control.

   c. Sweeps may be set at different sweep rates.

   d. When used with a 1A1 or modified CA, A Sweep is locked to Channel 1 and B Sweep is locked to Channel 2. (A-ALT-B mode only.)

   e. Two traces are displayed with single-trace plug-in.

   f. When used with dual trace plug-in in ALT DLY'D mode, the scope displays 4 traces or 8 traces with an M.

   g. BRIGHTNESS control (front panel screwdriver adj.) sets B unblanking level to balance trace intensity when the sweeps are running at different rates, and provide an adjustment for INTENSIFIED contrast in B INTENS BY A.

4. Single Sweep

   a. READY neons indicate when a sweep is armed and ready to accept a trigger.

   b. RESET controlled either by RESET position of SWEEP MODE switch or from EXT SINGLE SWEEP RESET.

5. Sweep Delay

   a. A DLY'D BY B can be alternated with B INTENS BY A.

   b. Socket on rear panel allows external time delay.

   c. Delayed trigger time jitter improved over 545A -- less than 1 part in 20,000.

   d. Delayed sweep time jitter improved over 545A -- less than 1 part in 20,000.

   e. Delay time multiplier is 10 turn HELIPOT.

6. External Horizontal Amplifier

   a. 1 - X10 variable control.

   b. X10 compensated attenuator.

   c. 1 meg at about 50 pf input Z.

   d. 450 KC passband.

   e. Sensitivity is about 80 mv/cm uncalibrated.

7. Triggering -- A and B Identical.

   a. Triggering our entire passband of scope.

   b. Trigger selectable from:

      (1) INT NORMAL.

      (2) INT PLUG-IN.

      (3) EXT.

      (4) LINE

   c. Coupling:

      (1) AC.

      (2) AC LF Rej.

      (3) DC.

d. ± Slope.

e. Automatic or Trig.

8. Outputs

a. A Gate, 25v.

b. B Gate, 25v.

c. A Sweep, 100v.

d. Delayed Trigger, 10v.

D. CRT

1. 5" round glass CRT, T5470.

a. Similar to 543.

2. 6 x 10 cm display area.

3. 10 kv accelerating potential.

4. Spot size nominally 9 mils.

5. Front panel electrical TRACE ROTATION.

6. Front panel ASTIGMATISM control.

7. INT, FOCUS, ASTIGMATISM and SCALE ALUMINATION controls on front panel have GRADUATED SCALES.

8. Z axis modulation (AC coupled) to the cathode.

9. DC unblanking.

E. Calibrator

1. 1 kc square wave.

2. .2 mv to 100v in 18 steps.

3. 50 ohm output Z at all millivolt steps.

4. 100v DC available.

5. 5 ma 1 kc square wave through a front panel current loop for calibrating current probes.

F. Power Supply

1. Will regulate from 103v to 130v.
2. -150v, +100v, +225v, +350v regulated supplies.
3. 325v unregulated DC available for HV oscillator.
4. Only 3 silicon stacks.
5. No separate transistor supply.
6. Switch places 750Ω, 25v load across 100v supply when plug-in out.
    a. Stays in regulation with plug-in out.
7. Conventional features such as fan, thermal overload relay, time delay relay.

TYPE 547

II. VERTICAL AMPLIFIER

A. The Vertical Amplifier provides the driving voltage for the CRT deflection plates.

1. The circuit also feeds a VERT SIG OUT jack.
2. A push-pull trigger take-off is provided.

B. Circuit Requirements

1. Output is a push-pull voltage of 7.2 v/cm* (CRT deflection factor).
   a. For 6 cm display, each plate must swing 21.6v*.
   b. Deflection plate voltage at screen center is 145v.
2. Input sensitivity is standardized at .1 v/cm push-pull.
   a. Elevated to 67.5v DC.
   b. Appears on pins 1 and 3 of the blue ribbon connector.
3. Nominal gain is 72.
4. Design safety factor requires vertical output capabilities three times the apparent requirements.
   a. 3 x 26.6v = 78v each plate.
   b. Each plate will swing from 100v to about 190v.
   c. Compression exceeds 5% above 170v.
5. Output signal current requirement is 27 ma.
   a. $I = C \frac{de}{dt}$

      where C is the deflection plate capacitance per plate plus collector capacitance, de is the voltage per plate for 4.8 cm (10% to 90% on a 6 cm graticule) and dt is the risetime of the system.

* Will vary with CRT deflection sensitivity.

b. $I = 10 \times 10^{-12} \quad \frac{17.25v}{6.25 \times 10^{-9}}$

$I = 27$ ma

6. VERT SIG OUT front panel jack.

   a. .35 v/cm minimum.

   b. Risetime 20 nsec min.

   c. Output Z is 230Ω.

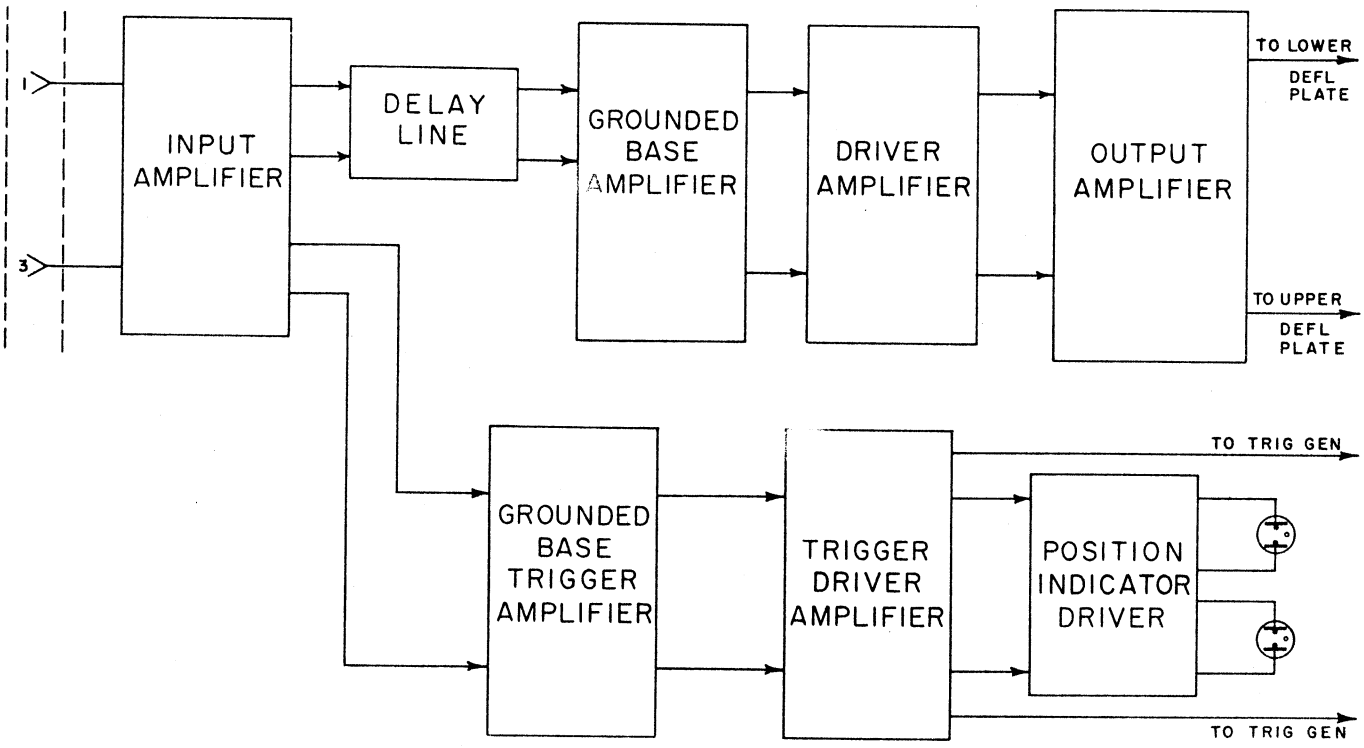
      (1) AC coupled through .02 μf cap.

7. Trigger signal to the A and B trigger generators

   a. Push-pull .7 v/cm.

   b. Output impedance is 93Ω.

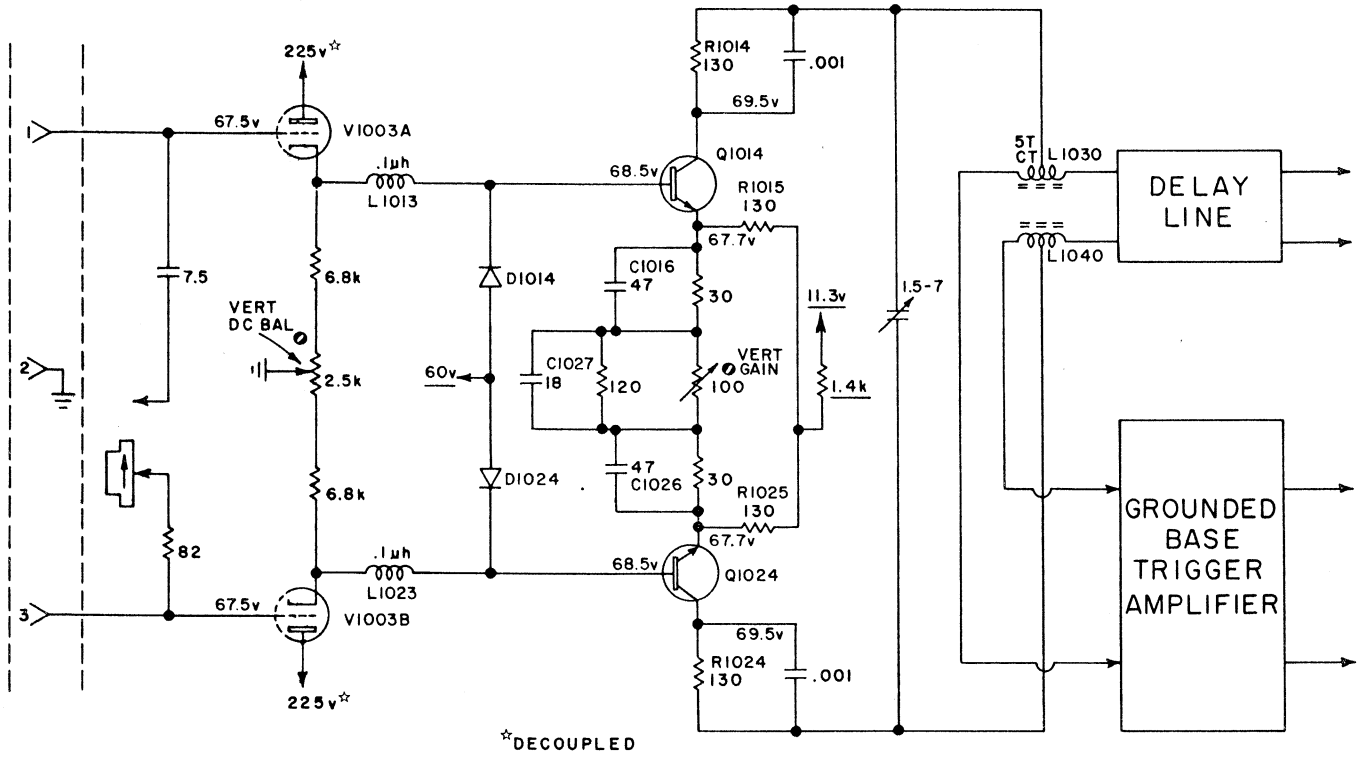
C. Block Diagram



TYPE 547 VERTICAL AMPLIFIER
BLOCK DIAGRAM

B-547-0037
3-20-'64 dl

D. Input Amplifier



TYPE 547 VERTICAL AMPLIFIER
INPUT AMPLIFIER

B-547-0038x
3-23-'64 dl

1. The circuit consists of a pair of cathode followers driving an emitter coupled push-pull amplifier.
   a. V1003A and V1003B are halves of a 12AT7.
   b. Q1014 and Q1024 are RCA 2N2475 silicon NPN transistors.
   c. D1014 and D1024 are GE 1N3605 silicon diodes.
2. The input must be compatible with the existing letter series plug-ins, but should not restrict the bandpass of the 1 series plug-ins.
   a. .1 v/cm input sensitivity and 67.5v DC level are compatibility features of all letter plug-ins.

b. Plug-ins like the Type N with high output impedance require high input Z.

(1) Input cathode followers provide the high input Z.

c. The letter series plug-in characteristics were not controlled above 30 mc.

(1) Used with a wide bandpass vertical amplifier like the Type 547 would result in ringing, overshoot, etc.

(2) A 7.5 pf capacitor and 82 ohm resistor are connected between pins 1 and 3 whenever a letter series plug-in is used.

(3) A switch, actuated by the plug-in, connects the R-C to the circuit.

(4) Plug-ins such as the Type 1A1 have a hole in the rear panel so the switch will not be pressed.

3. The cathode followers are not cathode coupled.

4. A VERT DC BAL control corrects for unbalance in the amplifier.

a. If the VERT POSITION control in the plug-in sets the level on pins 1 and 3 the same, the trace should be centered.

b. The VERT DC BAL control has a swing of about 8 cm to assure this DC balance without selecting transistors.

5. The CF is directly coupled to the push-pull amplifier bases.

a. L1013 and L1023 provide high speed peaking.

6. D1014 and D1024 are catching diodes that prevent Q1014 and Q1024 bases from dropping below 60v.

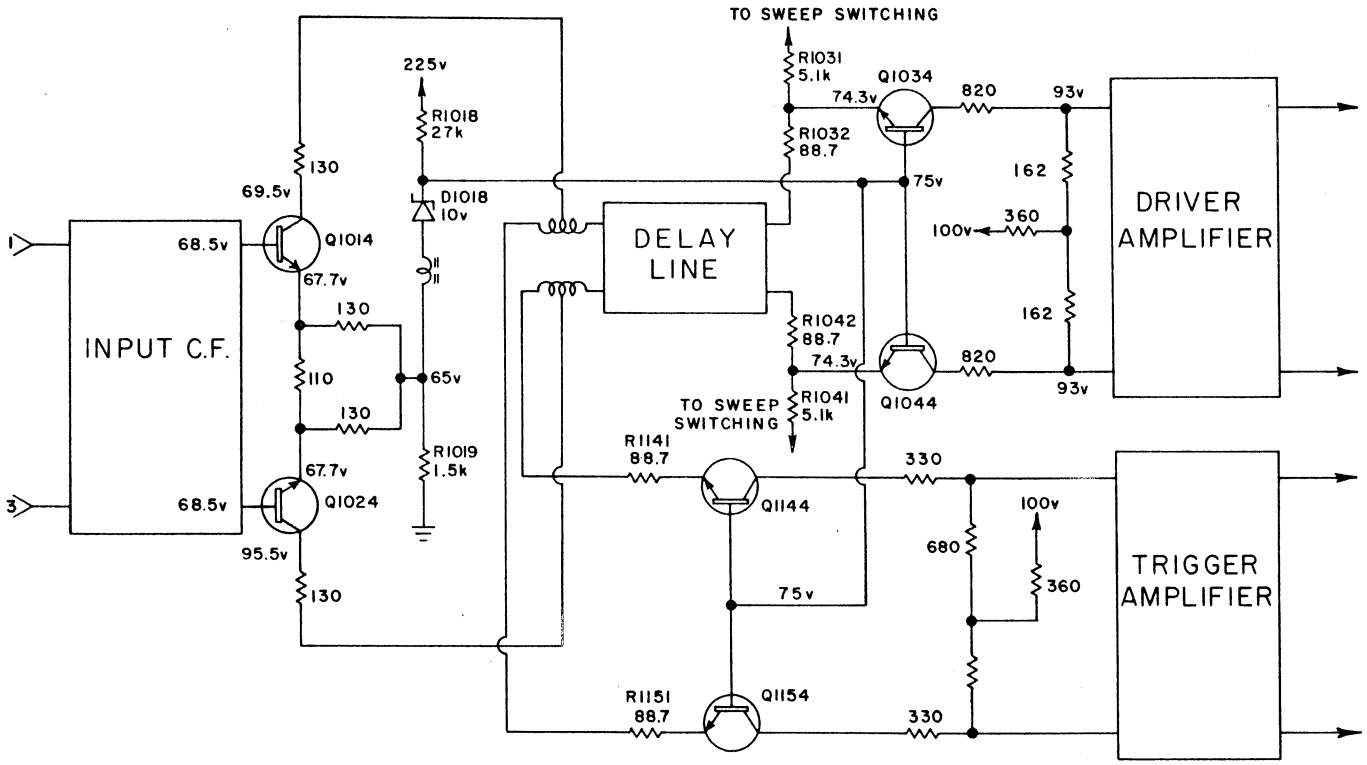
a. If the plug-in is removed when the scope is on (or V1003 is removed from its socket), the diodes catch the bases at 60v, preventing collector-base breakdown.

b. V_{CBO} for a 2N2475 is 15v.

7. Q1014 and Q1024 form an emitter coupled push-pull amplifier.
   a. VERT GAIN is adjusted by varying the coupling between the emitters.
      (1) Increased resistance increases degeneration and decreases gain of the stage.
   b. Emitter tying resistors are bypassed by C1016, C1026 and C1027 to provide HF peaking.
      (1) Degeneration is reduced at higher frequencies by capacitively tying the emitters together.
      (2) This scheme makes this peaking less variable with the gain.
   c. Emitter returns are through R1015, R1025 and through an equivalent 1.4k to 11.3v.
8. The collectors tie through R1014 and R1024 to the center tap of the Tee matching coils L1030 and L1040.
   a. Collector current flows through a rather complex load including the Tee coils, the Delay Line and both Grounded Base Amplifiers.
   b. Total collector resistance value is chosen to provide proper collector load for thermal compensation.*

* Reference story in appendix.

E. Input Circuits, DC Considerations



TYPE 547 VERTICAL AMPLIFIER
INPUT CIRCUIT DC LEVELS

B-547-0039x
3-25-'64 dl

1. The input push-pull amplifier drives the Grounded Base Amplifiers, which in turn provide a current drive to both the Vertical Driver Amplifier (Q1074 and Q1084) and the Trigger Driver Amplifier (Q1164 and Q1174).
2. A 170 nsec delay line delays the signal between the push-pull amplifier and vertical output.

a. A Tek made counter spiral wound shielded and encapsulated line is used.

b. No delay line adjustments are required.

c. The line has a characteristic impedance of 186 ohms (93 ohms each side).

d. .01 inch wire is used with a DC resistance of about 8 ohms.

3. The Delay Line must be terminated at both ends in 93 ohms.

a. In order to obtain a low terminating impedance, grounded base amplifiers are used.

b. The output impedance consists of 88.7 ohms, R1032 (and R1042) and the 5 ohm emitter impedance of the grounded base stage.

c. The input termination is made up of the 88.7 ohm R1141 (and R1151) and the 5 ohm emitter impedance of the grounded base amplifier in the Trigger Take-Off circuit.

4. Q1014 and Q1024 collector drives the center tap of the Tee coil.

a. Signal current is split equally in the Tee coil.

b. Half the current flows through the Delay Line and Q1034, Q1044.

c. The other half of the signal current flows through Q1144 and A1154.

5. The Grounded Base Amplifiers provide a high impedance current drive to following push-pull stages.

6. Although plug-in DC levels at pins 1 and 3 usually are standardized at 67v, there have been exceptions.

a. DC levels have varied from 65v to 72v.

b. A change in DC levels and subsequent current changes in Q1014 and Q1024 would upset the thermal compensation balance achieved by selection of collector load resistors.

7. A DC feedback circuit compensates for possible different DC levels at pins 1 and 3.

a. Q1034, Q1044, Q1144, Q1154 bases are tied to a divider composed of R1018 and R1019.

b. Emitter current from Q1014 and Q1024 pulls the top of R1019 up to 65v.

(1) 19 ma static current flows in each transistor.

c. This level is raised by D1018 (10v zener) to 75v.

d. If the input DC level should increase (for example), Q1014 and Q1024 emitters would raise.

e. The DC level on the Grounded Base Amplifier bases would raise an equal amount.

f. Q1034, Q1044, Q1144, and Q1154 act as emitter followers, bootstrapping Q1014 and Q1024 collectors to a level compatible with their emitters.

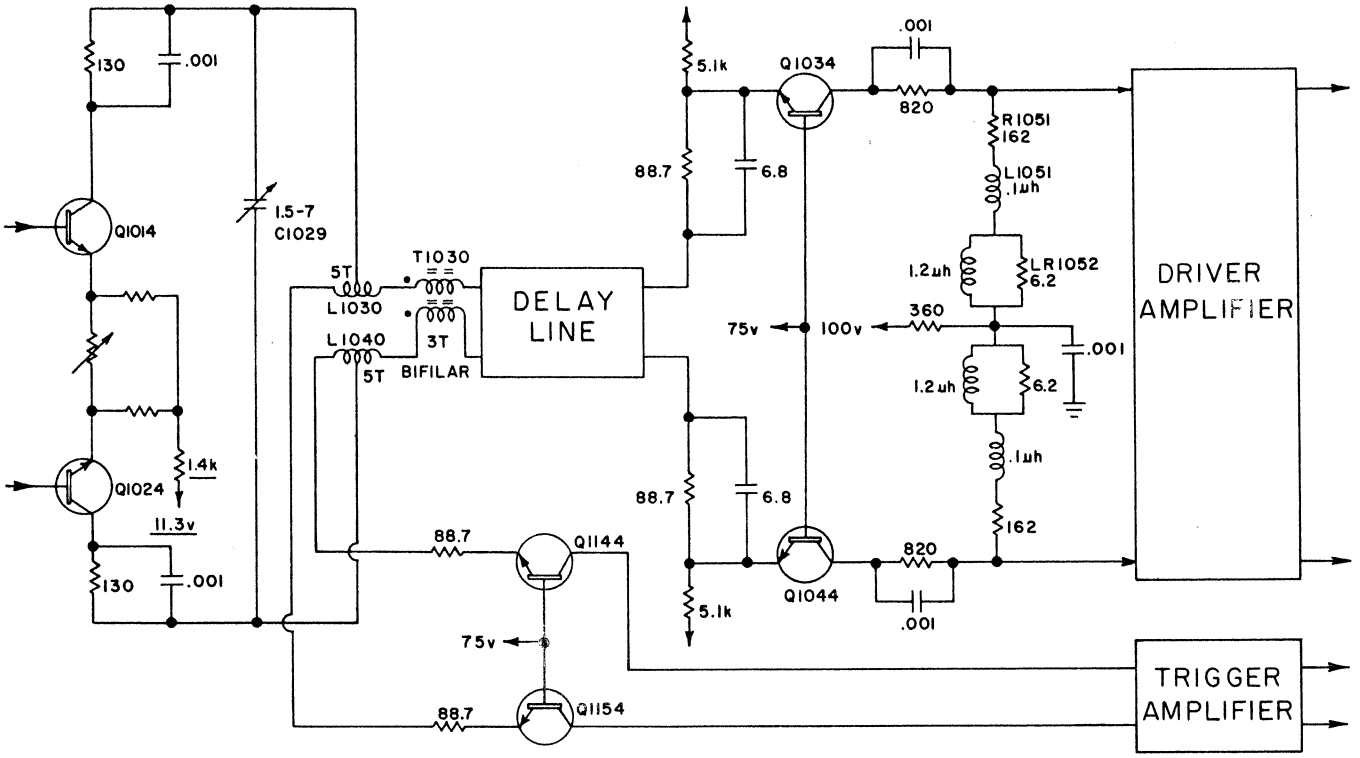
8. Currents from the TRACE SEPARATION circuit may flow through R1031 and R1041.

a. In all HORIZONTAL DISPLAY modes except the two ALT modes, no current flows through the 51k resistors.

b. When in the ALT modes and while A sweep is displayed, positioning current through R1031 and R1041 will position the trace.

c. A maximum of ±4 ma can flow through each resistor, depending on the position of the TRACE SEPARATION control.

F. Input Circuits, AC Consideration



TYPE 547 VERTICAL AMPLIFIER
GROUNDED BASE AMPLIFIER, DELAY LINE

B-547-0040x
3-26-'64 dl

1. T1030 provides a high impedance path for common mode AC signals.
   a. Common mode signals can originate from transistor or component unbalance in the push-pull input amplifier.
   b. The inductor consists of 3 turns on a ferrite core.
   c. Push-pull signals pass unimpeded.

2. Tee coils, L1030 and L1040, appear as a section of transmission line.

   a. C1029 tunes the line to 186 ohms.

3. C1031 and C1042 compensate for an inductive effect at Q1034, Q1044 emitters.

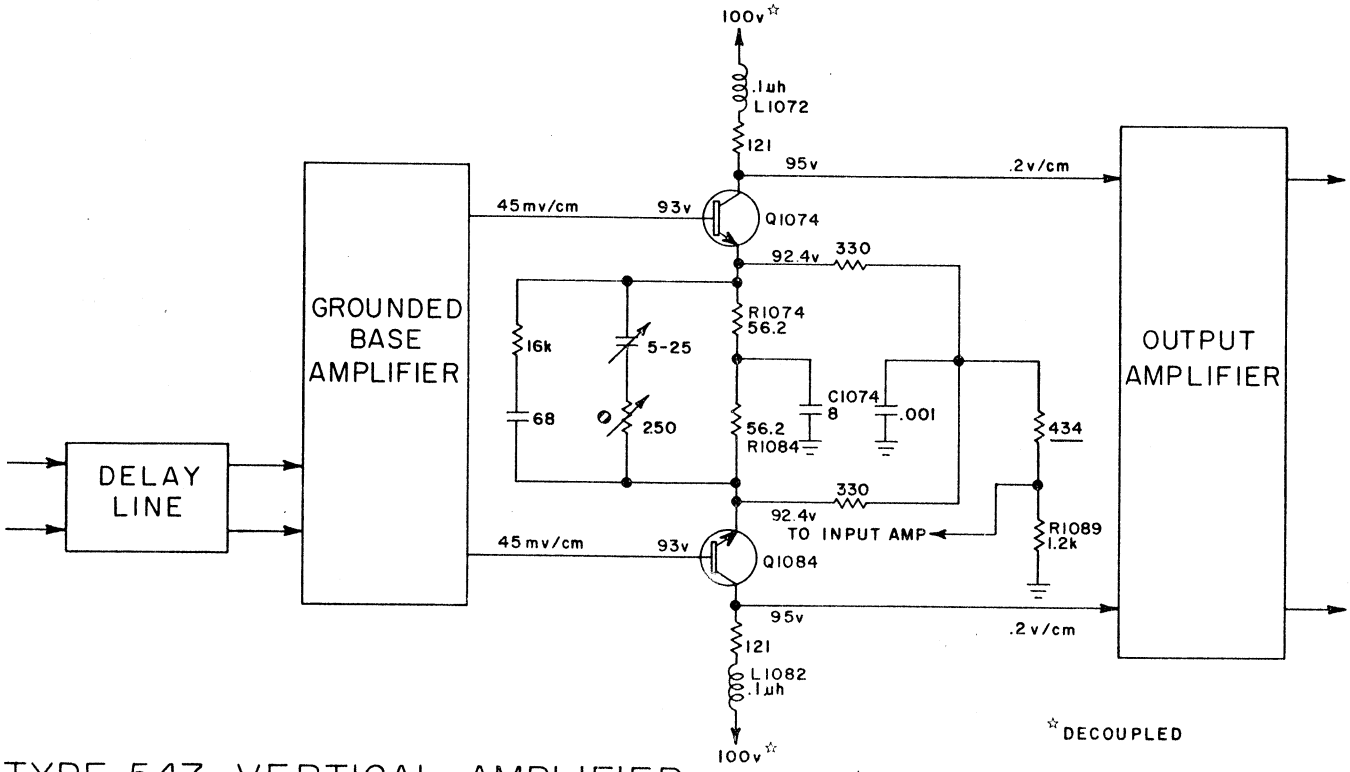
4. Although dribble-up* occurs to a step passing through the delay line, no single compensating circuit is designed to correct it.

   a. Compensating networks with different time constants correct for various risetime degradations including dribble-up.

   b. The L/R networks composed of R1051, L1051, LR1952 and the complementary set of components, contribute to this risetime compensation.

5. Signal level at the delay line is about 50 mv/cm.

G. Driver Amplifier



TYPE 547 VERTICAL AMPLIFIER
DRIVER AMPLIFIER

B-547-0041x
3-27-'64 dl

* See Nanosecond Pulse Measurements, by C. N. Winningstad.

1. The Driver Amplifier is a transistorized emitter coupled push-pull amplifier.
   a. Q1074 and Q1084 are 2N2475 silicon transistors.
2. The transistors operate Class A.
   a. Q1074, Q1084 bases, 93v.
   b. Q1074, Q1084 emitters, 92.4v.
   c. Q1074, Q1084 collectors, 95v.
3. Emitter tying resistors, R1074 and R1084 introduce some degeneration.
   a. Degeneration is bypassed at high frequencies by two RC networks to provide HF peaking.
   b. These networks are part of the compensation required to build up the leading edge of a unit step through the amplifier.
   c. The emitter coupling provides cancellation of any common mode signal that might be present.
   d. C1074 breaks up a 300 mc oscillation.
      (1) A capacitor in this position would prevent common mode rejection.
      (2) Any common mode signal not rejected because of this capacitor would be beyond the range of the amplifier.
4. The tapped emitter current supply provides a convenient source of 60v for the base catching diodes in the Input Amplifier.
   a. The circuit is decoupled so no AC feedback occurs.
   b. There is a DC change in the emitter supply, however, when a plug-in is removed.

c. As D1014 and D1024 (Input Amplifier) conduct, the top of R1089 drops about 3v as current is diverted through the diodes.

d. This provides some stabilizing of DC levels in Q1074 and Q1084.

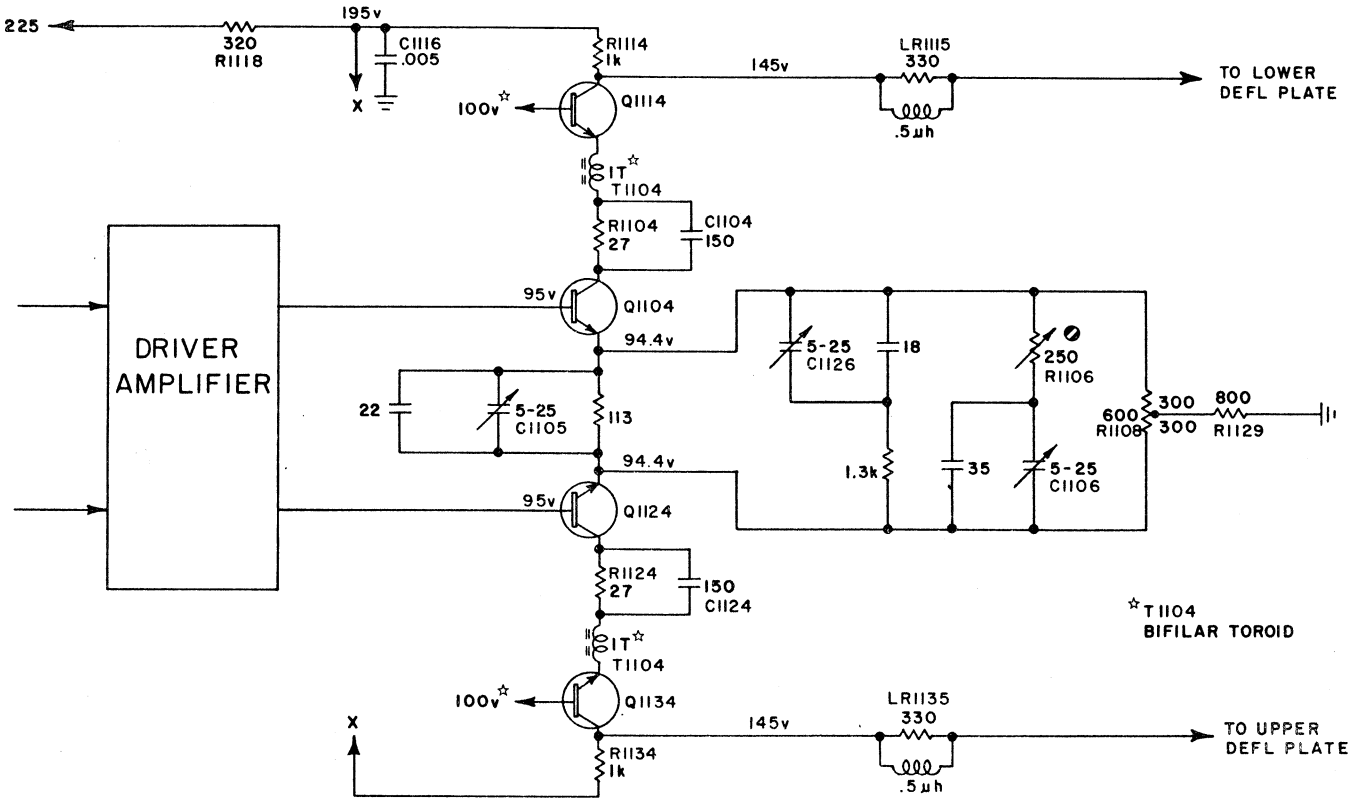
e. A side effect of the DC bootstrap action through the Grounded Base Amplifier is to raise their collectors and the bases of Q1074 and Q1084.

5. Shunt peaking is provided by L1072 and L1082 as part of the collector loads.

6. Signal level at Q1074 and Q1084 bases is 45 mv/cm and on the collector, .2 v/cm.

H. Output Amplifier

1. The Output Amplifier is an emitter coupled cascode push-pull amplifier.



TYPE 547 VERTICAL AMPLIFIER
OUTPUT AMPLIFIER

B-547-0042
3-30-'64 dl

2. The circuit uses four transistors.

   a. Q1104 and Q1124 are Fairchild 2N2369 silicon NPN transistors.

      (1) 400 mc Ft.

   b. Q1114 and Q1134 are RCA TA1938 silicon NPN transistors (151-124 will substitute).

      (1) 310 mc Ft.

3. Quiescent levels (trace centered), Q1104, Q1124, Q1114, Q1135.

   a. Q1104, Q1124 bases, 95v.

   b. Q1104, Q1124 emitters, 94.4v.

   c. Q1104, Q1124 collectors, 99v.

   d. Q1114, Q1134 collectors, 145v.

4. A cascode amplifier provides a method of achieving a relatively large voltage gain with no appreciable Miller capacitance.

   a. The drive from the Drvier Amplifier (Q1074 and Q1084) has a 121 ohm collector load impedance.

   b. If Q1104 and Q1124 collectors were required to deliver the full deflection plate voltage (if cascode circuit not used) Miller capacitance would load the driving circuit.

      (1) Average input C for a 2N2369 is 2.8 pf.

      (2) Miller capacitance = C (1 + A).

          Cm = 2.8 pf (1 + 18).

          Cm = 53 pf.

      (3) Rt = 2.2 RC where R is the driving collector impedance and C is the Miller capacitance.

(4) Rt = 2.2 x 121 x 53 pf.

Rt = 14 nsec.

(5) This risetime exceeds the 6.25 nsec requirement for the amplifier.

c. By current driving Q1114 and Q1134 emitters, Q1104 and Q1124 collectors have little voltage swing.

(1) Q1104, Q1124 collectors swing about 120 mv/cm.

(2) The lower impedance Q1114 and Q1134 emitters swing 6 mv/cm.

d. No Miller capacitance is present.

5. Q1104, Q1124 bases are each driven by a .2 v/cm signal.

6. 3.6 ma/cm is developed in each cascode circuit.

7. The signal voltage taken across collector load resistors, R1114 and R1134, is the 7.2 v/cm deflection plate push-pull driving voltage.

a. R1114 and R1134 are Tek made controlled-inductance resistors.

8. The signal current requirement for a fast step is an additional 27 ma to charge deflection plate capacitance 17.25 volts in 6.25 nsec.

a. The current requirement is satisfied by the various RC networks between Q1104 and Q1124 emitters.

b. Time constants have "staggered" values to shape the leading edge of the unit step.

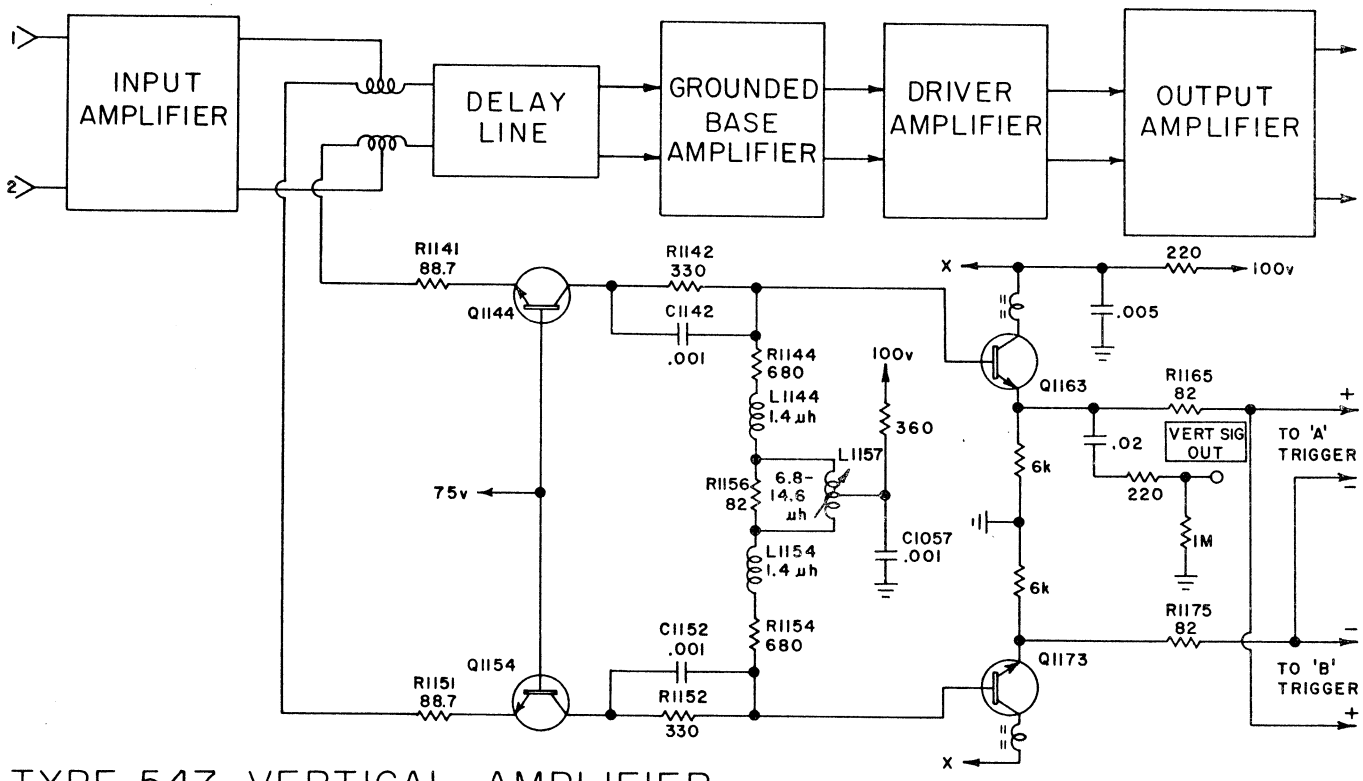
c. C1126, C1105, C1106 and R1106 provide tweeking adjustments.

9. Emitter current for the cascade amplifier flows through the Tek made center tapped R1108 and R1129.
   a. About 50 ma quiescent current flows through each transistor.
   b. R1105 has very low inductance, will dissipate heat well, and fits nicely on the PC board.
10. T1104 presents a high impedance to very high frequency common mode signals.
   a. A high frequency oscillation is prevented.
   b. T1104 is a bifilar winding on a toroid.
   c. Push-pull signals are not affected.
11. R1104 and R1124 (along with Q1114, Q1135 emitter impedance) provide a proper collector load to set Q1104 and Q1124 maximum power point for temperature stabilization.*
   a. C1104 and C1124 tie Q1104, Q1124 collectors to the low impedance emitters of Q1114 and Q1134 at high frequencies.
   b. If the collectors are tied to a low impedance point at high frequencies, Miller capacitance cannot develop.
12. R1118 and C1116 provide a decoupled common 195v supply for the cascode stage.
13. RL1115 and RL1135 separate the collector capacitance from deflection plate capacitance.
   a. Low Q series peaking is provided by the L/R.

* See reference story in appendix.

I. Trigger Amplifier

1. The Trigger Amplifier provides a push-pull trigger signal to both the A and B trigger circuits.
2. A single ended VERT SIG OUT signal is fed to a front panel jack.
3. Q1163 and Q1164 are Fairchild 2N2369 silicon transistors.



TYPE 547 VERTICAL AMPLIFIER
TRIGGER AMPLIFIER

B-547-0043x
3-31-'64 dl

4. The 100 mv/cm push-pull signal at a DC level of about 70v is applied to the emitters of the Common Base Amplifier, Q1144 and Q1154.
   a. The Common Base Amplifier provides a low terminating impedance for the delay line and a high impedance drive to the output emitter followers.
   b. R1141 and R1151, with the emitter impedance of the Common Base stage, terminate the delay line in 93 ohm (186 ohm push-pull).
5. R1142 and R1152 provide the proper collector load to operate the transistors at the maximum power point for temperature compensation.
   a. C1142 and C1152 offer a path for AC signals.
6. L/R networks composed of R1144, L1144, R1154, L1154, R1156 and L1157 help shape the leading edge of a step.
   a. L1157, a center tapped inductor provides variable adjustment to both sides of the push-pull signal.
7. Q1163 and Q1173 are emitter followers driving the trigger circuits, the VERT SIG OUT jack and the Indicator Neon Driver.
   a. There is no emitter coupling.
   b. Toroid inductors in each collector lead suppress oscillation.
   c. R1165, R1175 and the emitter resistance comprise the 93 ohm output impedance to the trigger generator.
8. The VERT SIG OUT signal is 350 mv/cm.
   a. Output impedance is 230 ohms.
   b. AC coupled through a .02 μf.
   c. 3 db down at 8 cps.

9. A glitch appears on the VERT SIG OUT waveform (on early instruments).

   a. It occurs during hold-off time for both sweeps.

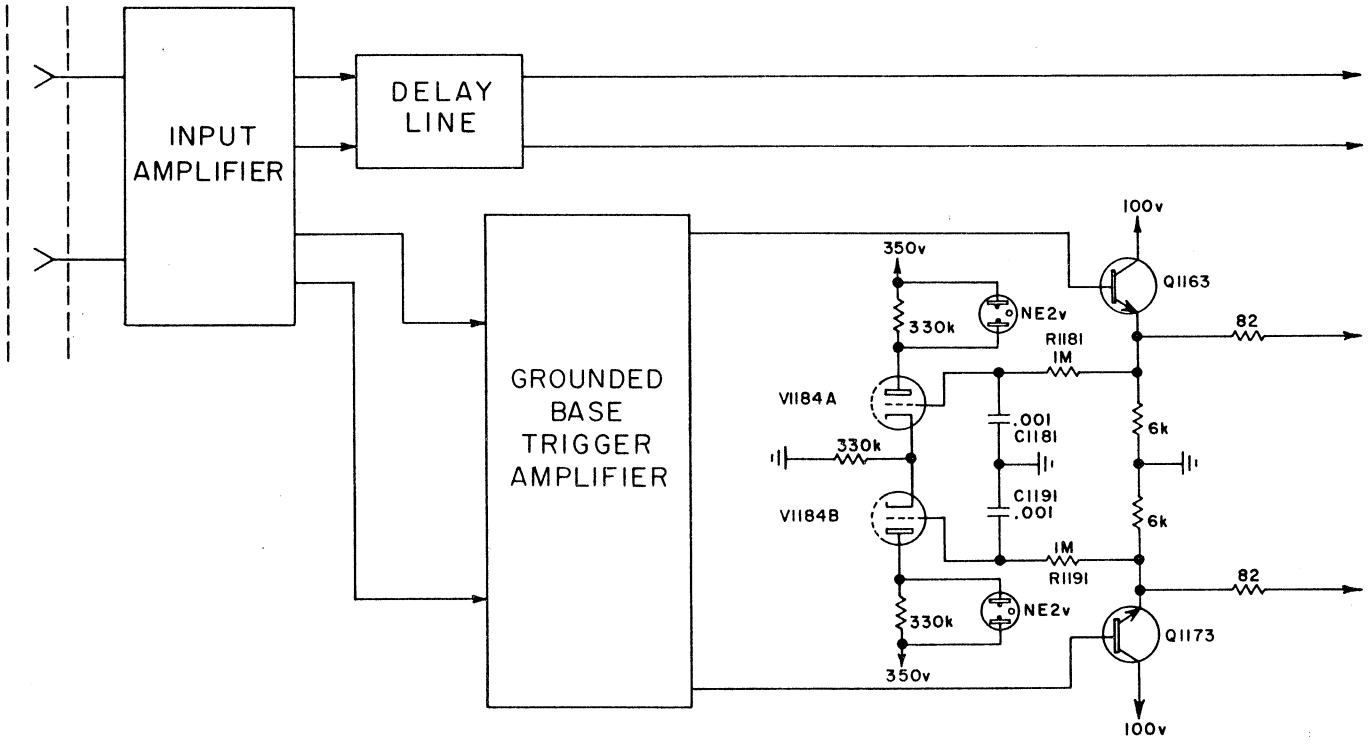
   b. The glitch comes from the Hold-Off Multi through the 100v bus.

   c. It is also present at Q1074, Q1084 bases, but as a common mode signal is rejected in the emitter coupling.

   d. Increasing C1057 to .1 μf will reduce the aberration if objectionable.

J. Neon Indicator Driver

1. The indicator neons indicate the position of the trace (above or below the screen).



TYPE 547 VERTICAL AMPLIFIER
INDICATOR NEON DRIVERS

B-547-0044x
4-1-'64 dl

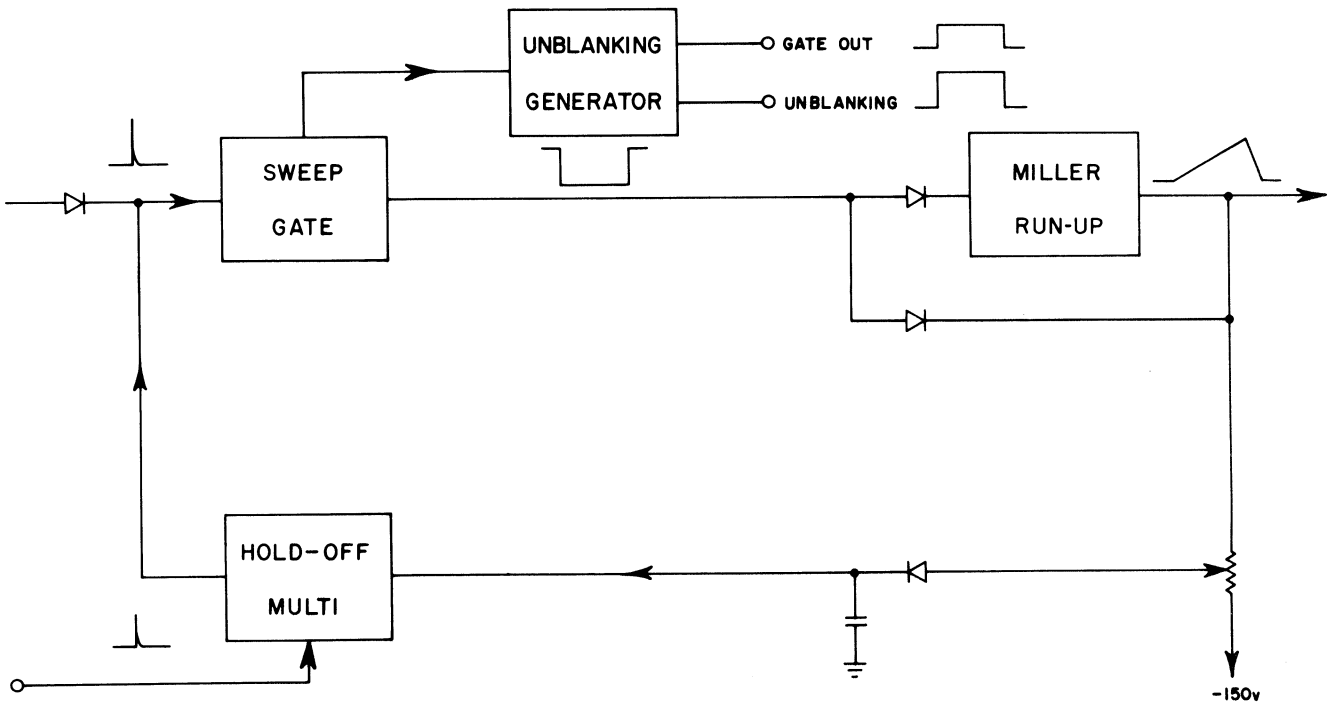
2. The upper neon must ignite before the beam moves more than 2 cm above screen center.
   a. The lower neon lights just before the beam drops 2 cm below the screen center.
   b. They fire at about 300v.
3. The Neon Drivers are two halves of a 12AX7 dual triode.
4. The neons are NE2V's.
5. A 1 ms time constant composed of R1181, C1181 and R1191, C1191 keep the grids from following fast signal changes.
   a. The neons light only when DC or slow AC changes move the beam to the top or bottom of the graticule.
6. A plastic cover prevents the otherwise exposed neon sockets from being a shock hazard.

III. SWEEP GENERATORS

A. Basically, the A and B Sweep Generators are alike although the B is considered the main sweep.

1. Identical sweep speeds.
2. Both generate 100v linear sweep ramp.
3. Both produce 25v GATE waveforms to front panel jacks.
4. Both generate unblanking waveforms.
5. A Sweep Generator has SWEEP OUT waveform to a front panel jack.
6. B Sweep Generator feeds a 100v ramp to the Delay Pickoff.

B. Block Diagram



TYPE 547 SWEEP GENERATOR
BLOCK DIAGRAM

B-547-0010
3-24-64 jg

C. Basic Circuits

1. Sweep Gate
2. Miller Run-Up
3. Hold-Off Multi
4. Disconnect Diodes
5. Unblanking Generator
6. Auto Multi
7. Ready Light Circuit

D. Improvements Over 545A

1. Simpler controls.
2. Faster time from trigger to start of sweep.
3. Smaller physical circuit layout - solid state circuitry where practical.
4. Lower power requirements - transistors.
5. Better reliability - transistors - precision resistors.
6. Better stability - TD Sweep Gating Multi, Hold-Off Multi.
7. Bright-Line Automatic.
8. Circuits adaptable to Sweep Switching.

E. Block Logic

1. A positive going trigger flips the Sweep Gating TD to its high state.
2. The positive step generated by the TD is amplified and inverted in the Sweep Gating circuit and applied to the disconnect diode, D286.
3. D286 cuts off, allowing the Miller tube to begin its sweep ramp.
4. The positive going ramp thus generated is fed to the Horizontal Amplifier.

5. A portion of the ramp is picked off the Sweep Length control and fed to the Hold-Off Multi.
6. When the sweep has reached sufficient length, the Hold-Off Multi flips.
7. As the Hold-Off Multi flips, it switches the Sweep Gating TD to a low state that cannot be influenced by a trigger.
8. The Disconnect Diode conducts and retrace starts.
9. At the start of retrace, the Hold-Off Diode opens.
10. The Hold-Off circuit delays the fall of the waveform, allowing retrace to become completed and the sweep circuits to become recovered.
11. At the end of hold-off, the Hold-Off Multi flips, switching the Sweep Gating TD to its triggerable condition.

F. Sweep Timing Switches

1. The A and B Sweep Timing switches, switch, timing resistors, timing capacitors, hold-off resistors and hold-off capacitors.
2. The and A and B timing switch circuits are the same in most respects.
    a. The A Switch circuit has an A SWEEP CAL control.
    b. The A Switch circuit includes hold-off correction resistors, R330A, R330B, R330C and R330D that can be connected to 350v (by the HORIZONTAL DISPLAY switch) while in the DLY'D and INTEN modes.

3. A VARIABLE control is provided for both A Sweep and B Sweep (VARIABLE TIME/CM).

   a. The controls provide a variable increase of at least 2.5:1 (typically 3:1) over the calibrated sweep ranges.

   b. An UNCAL lamp is provided for each sweep that lights when the VARIABLE knob is turned away from its calibrated position.

      (1) The calibrated position is also indicated by a detent (a cap switch).

4. Sweep Timing components.

   a. Timing caps.

      (1) Timing positions from 1 sec to 5 sec use 10 μf Tek made mylar caps.

      (2) Positions .1 sec to .5 sec use 1 μf Tek made mylar caps.

      (3) Positions 10 msec to 50 msec use .1 μf Tek mylar caps.

      (4) Positions 1 msec to 5 msec use .01 μf Tek mylar caps.

      (5) Positions .1 msec to .5 msec use .001 μf Tek mylar caps.

      (6) Positions from .1 μsec to 50 μsec use variable caps.

   b. Timing resistors.

      (1) The timing resistors used in the 5 sec, .5 sec, etc., positions are matched pairs (A and B Sweep) of 7M, 1% pyrofilm resistors.

      (2) All other timing resistors are 1% metal film resistors.

      (3) The switch grounds the top of all timing resistors not in use.

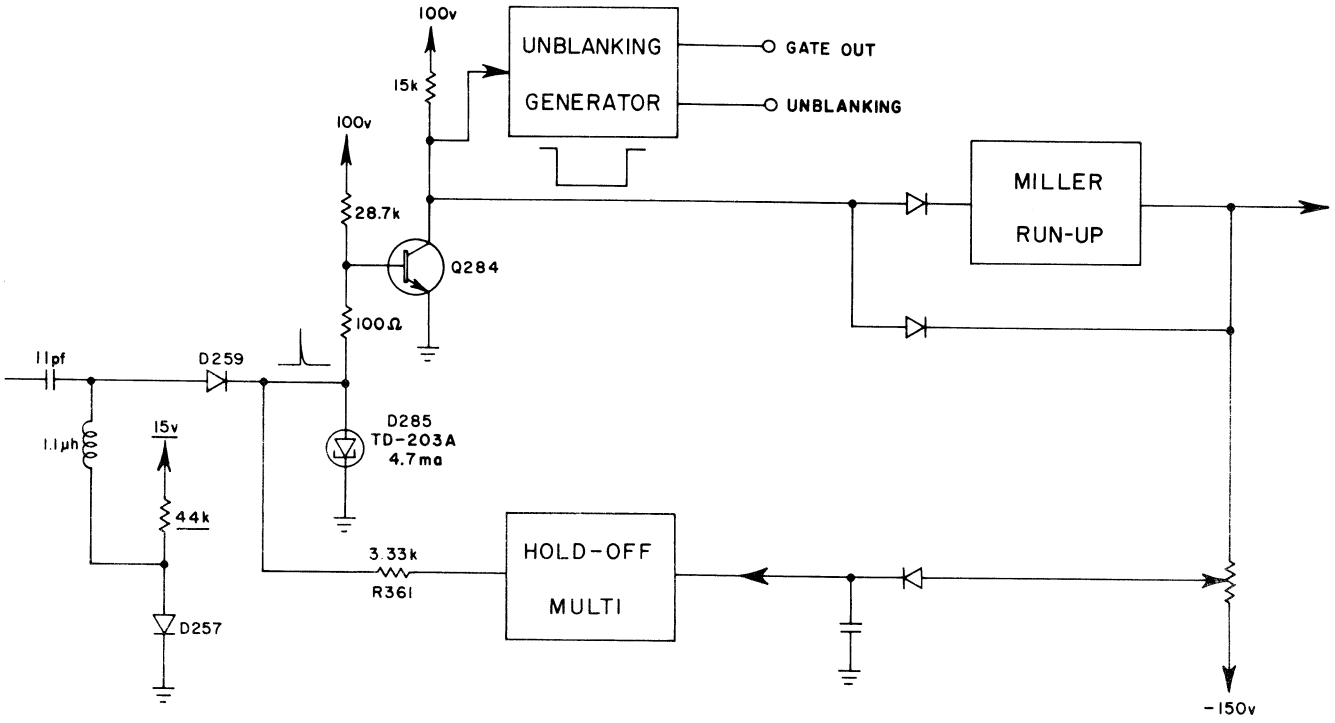
(4) A constant load for the VARIABLE control is maintained in all switch positions.

c. Hold-off capacitors are 10% tubular caps.

IV. A SWEEP GENERATOR

A. Sweep Gate

1. The Sweep Gate provides a negative going step to initiate sweep and a positive going step to stop it.



TYPE 547 SWEEP GENERATOR A
SWEEP GATE CIRCUIT

B-547-0011x
3-24-'64 jg

2. The circuit consists of a tunnel diode and one transistor.

   a. D285 is a GE TD-203A* 4.7 ma tunnel diode.

   b. Q284 is a Motorola 2N2501 silicon NPN transistor.

* See curve in appendix.

3. The TD has three operating conditions influenced by the Hold-Off Multi and the incoming trigger.

   a. Triggerable state - the TD is in its low state with 4.1 ma forward current.

   b. High state - 4.7 ma of forward current will flip it to the high state with about 500 mv drop across the diode.

   c. Locked out (low state) with 2.2 ma reverse current.

4. Quiescent (triggerable) condition:

   a. The Hold-Off Multi output is setting at 1.5v.

   b. 4.1 ma forward current flows through the TD.

      (1) .6 ma flows through R361 to the Hold-Off Multi.

      (2) 3.5 ma flows through R282.

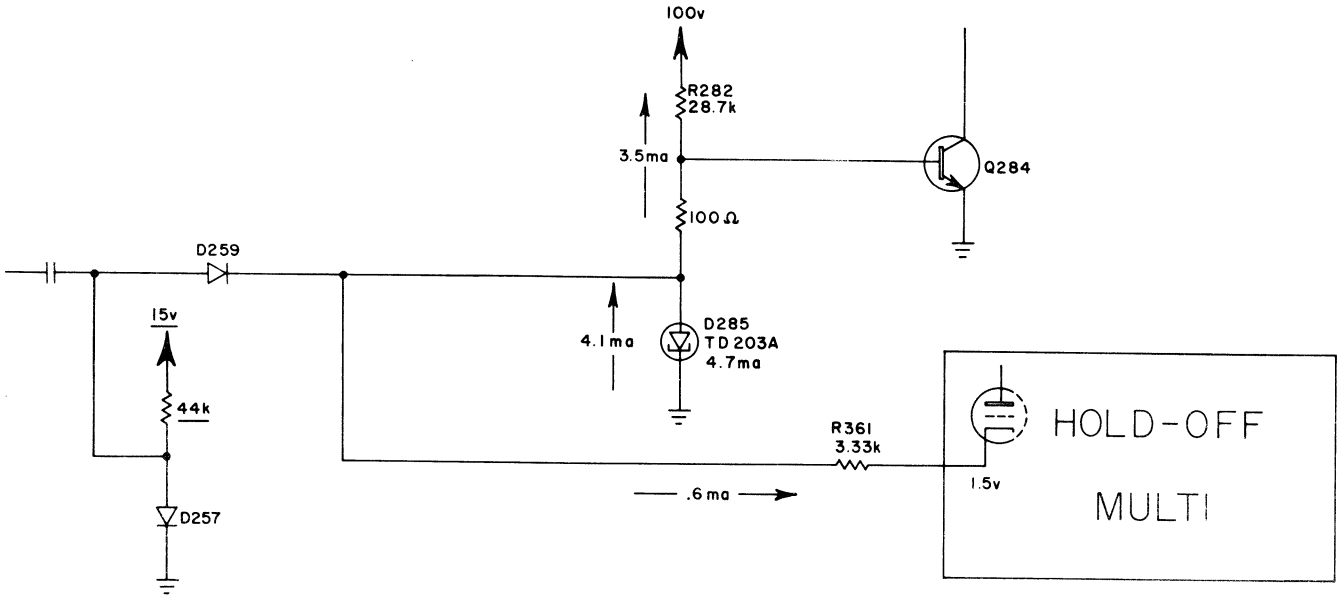
   c. Q284 collector sets at 5.4v.

   d. D259 is held on the edge of conduction by voltage setting D257.

5. A positive trigger will lift D259 into conduction.

a. The diode current added to the 4.1 ma already flowing through the TD will flip it to its high state.

b. Only 600 μa is required to bring the TD to its rated 4.7 ma.



TYPE 547 SWEEP GENERATOR A
SWEEP GATE CURRENT DISTRIBUTION

B-547-0011.lxx
4-8-'64 jg

6. As the TD flips to its high state, Q284 saturates.

   a. The collector drops to 0v (from 5.4v).

   b. The negative step cuts off D286 starting sweep.

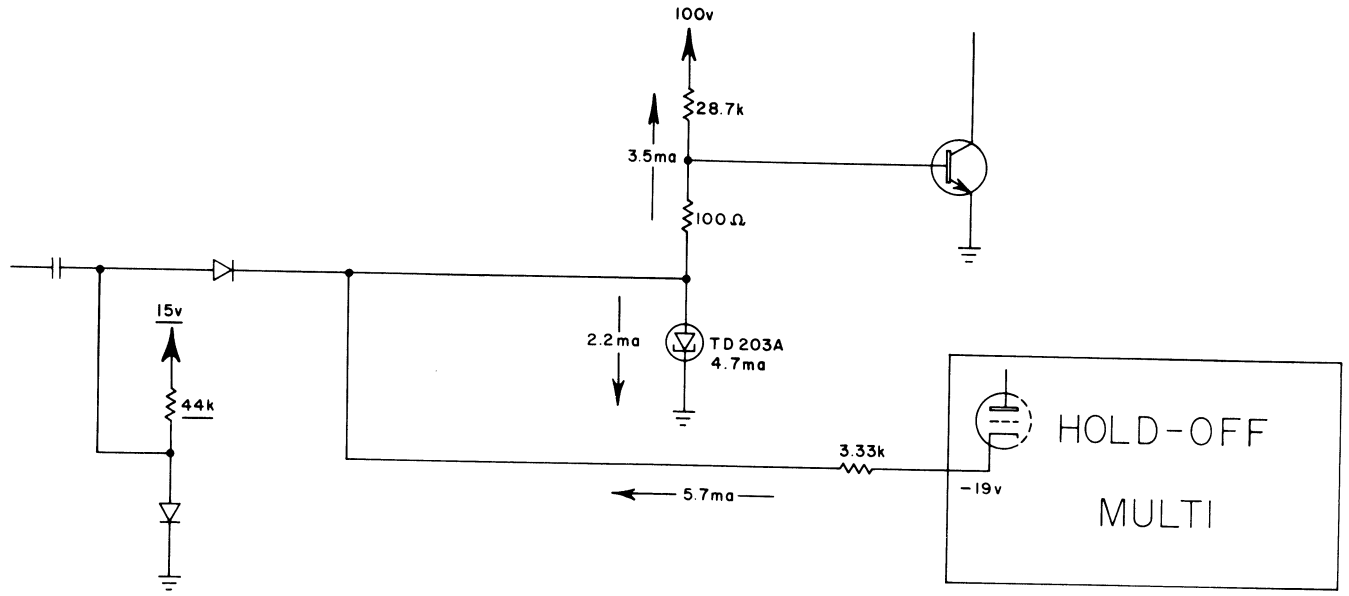
   c. The negative step is also fed to the Unblanking Amplifier.

7. At the end of trace, the Hold-Off Multi output drops to about -19v.

   a. 5.7 ma now flows through R361 from the Hold-Off Multi.

b. 2.2 ma of reverse current through D285 flips it to its low (locked out) state.

c. A trigger cannot flip the TD to its high state.



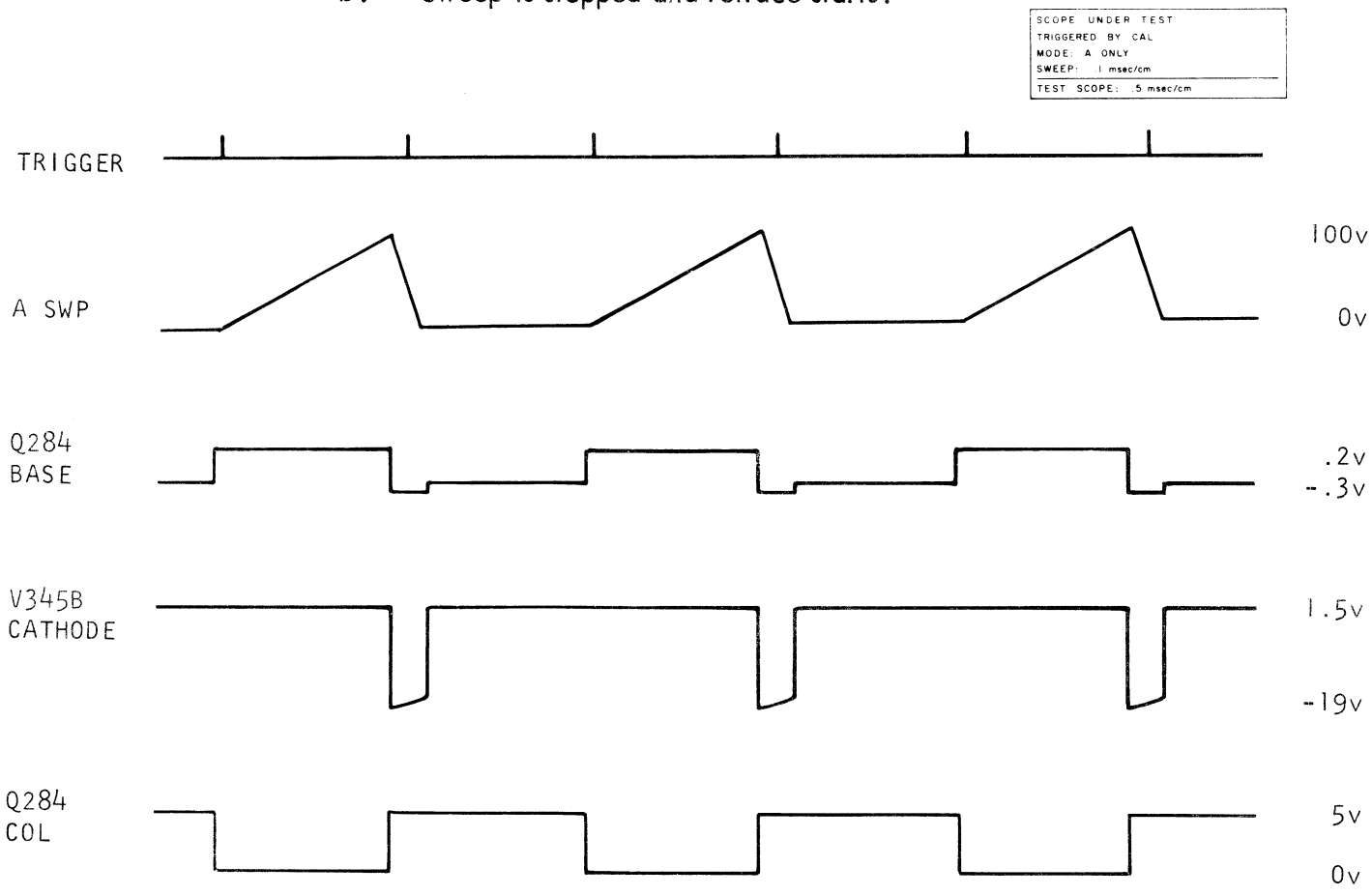
TYPE 547 SWEEP GENERATOR A
SWEEP GATE CURRENT DISTRIBUTION

B-547-0011.1x
4-8-'64 jg

8. As the TD flips to its low state, Q284 returns to its quiescent condition.

   a. As Q284 collector raises to 5.4v, D286 conducts.

   b. Sweep is stopped and retrace starts.



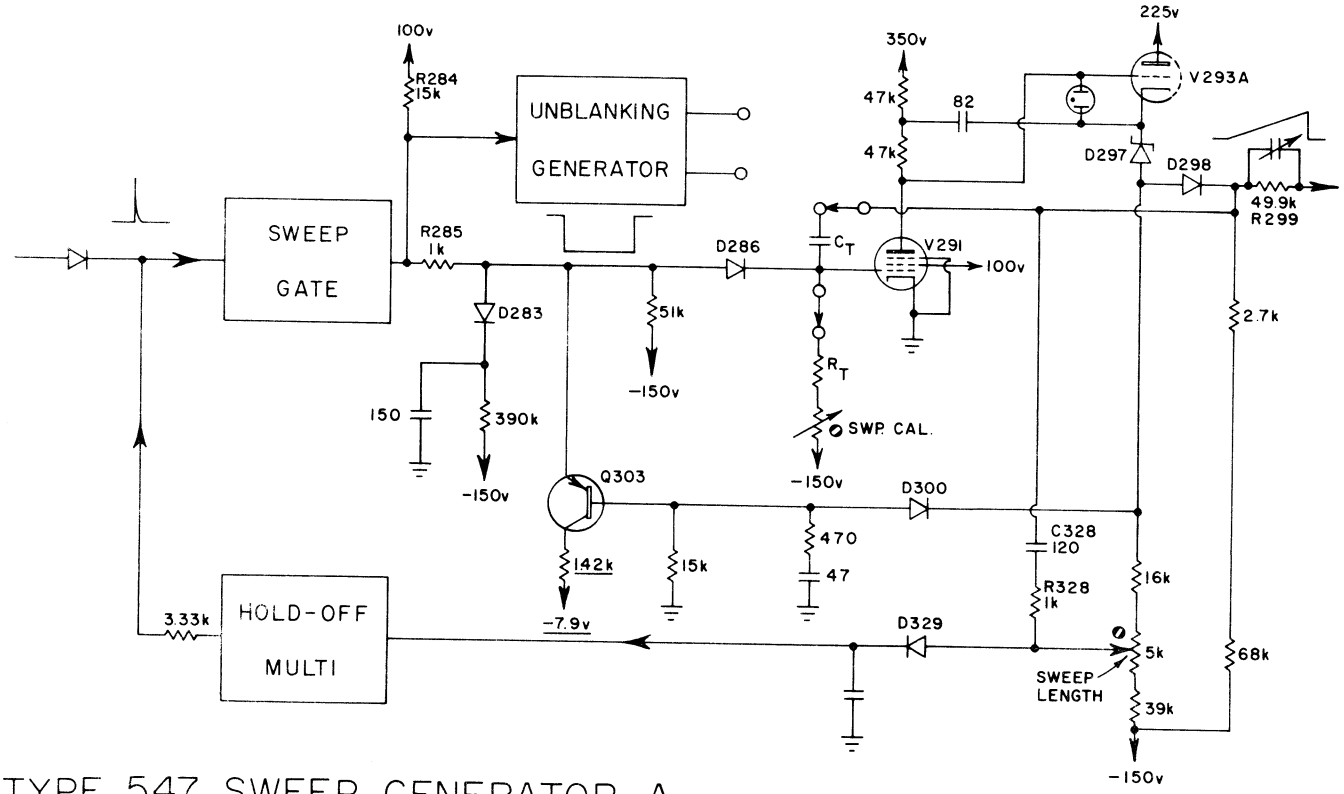
9. At the end of hold-off, the Hold-Off Multi output returns to 2.15v.

   a. With .6 ma flowing to the Hold-Off Multi, the TD returns to its forward biased low state.

   b. A trigger will start a new cycle.

B. Miller Run-Up

1. The Miller Run-Up supplies the sweep ramp to the Horizontal Amplifier and the SWEEP A voltage to a front panel jack.



TYPE 547 SWEEP GENERATOR A
MILLER RUN-UP

B-547-0012x
3-25-'64 jg

2. The Miller circuit uses a 6AU6 tube, a half 6DJ8, a transistor, four diodes and a zener.

   a. The Miller tube (V291) is a 6AU6 pentode.

   b. The run-up cathode follower is 1/2 6DJ8.

   c. Q303 is a Motorola 2N962 germanium PNP transistor.

   d. D286 is a Tek made GaAs diode.

e. D283 is a Type 6075.

f. D300 and D398 are Type 6061 silicon diodes.

g. D297 is a Motorola 1N3033 20%, 36v zener.

3. In the quiescent state, the tubes, diodes and the transistors are conducting.

a. V291 grid sets at -.5v.

b. V291 plate is at about 23v.

c. The output at D298 is at 0v.

4. A DC feedback loop composed of D286, V291, V293A, D300 and Q303 assure a consistant, stable starting potential for the sweep.

a. By using Q303 as a current amplifier, only the base current needs to be switched by D300.

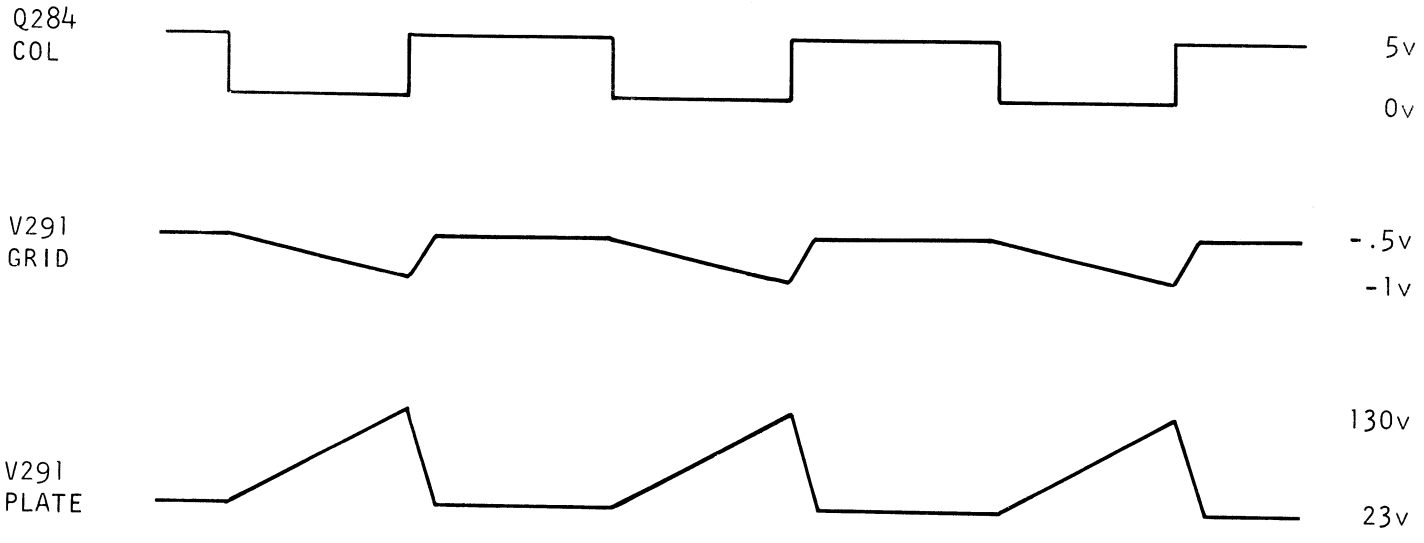
b. Actual clamping current flows through Q303 collector.

c. A step at the beginning of fast sweeps is minimized.

5. The 5.4v negative step from the Sweep Gate cuts off the Disconnect Diode (D286), Q303 and D283.

6. Sequence of operation at start of sweep:

a. With D286 open, the Miller tube grid starts toward -150v, charging the timing cap (C_T) through the timing resistor (R_T).



(1) Different values of precision timing resistors and precision Tek made timing capacitors are switched with each time/cm range.

b. The Miller tube plate begins to run up.

c. The ramp waveform is fed back to the top of the timing capacitor.

d. The positive going change at the top of the capacitor opposes the change at the bottom of the capacitor.

e. As a result of the feedback action, the Miller tube grid runs down less than 500 mv.

f. Since the voltage drop across the timing resistor remains virtually the same, the charging current into C_T remains constant.

g. Because a constant charging current into a capacitor results in a linear ramp of voltage across the capacitor, the output ramp is linear.

6. V293A provides a low impedance to charge C_T and to drive the SWEEP OUT CF.

a. B294 protects the tube should V291 open or be removed from its socket.

b. D297 allows normal operating plate voltage for the Miller tube (V291) when the output DC level is 0v.

7. Bootstrap capacitor, C294, improves gain at high sweep speeds and assures sweep linearity.

8. Sequence of operation at the end of sweep:

   a. The positive step from the Sweep Gate turns on D286 and Q303 after a brief delay.

      (1) With D283 conducting, C283 must charge before D286 anode can lift into conduction.

      (2) The delay in stopping sweep allows unblanking to end before retrace starts.

   b. When D286 conducts, the Miller tube grid raises to its quiescent condition.

   c. The Miller tube plate pulls down and retrace starts.

   d. C_T discharges through D286, R285 and R284 to 100v.

   e. D298 disconnects, allowing retrace to continue while the loop composed of D300, Q303, D286, V291 and V293A becomes connected.

      (1) The Miller circuit and the clamping loop reach their stable quiescent condition before retrace is finished.

9. The positive going output sweep ramp rises from 0v to about 105v to drive the Horizontal Amplifier.

   a. The Horizontal Amplifier is an operational amplifier.

   b. R299 is R_{in} for the Operational Amplifier.

   c. The output, as it feeds through the 50Ω coax, is a current waveform.

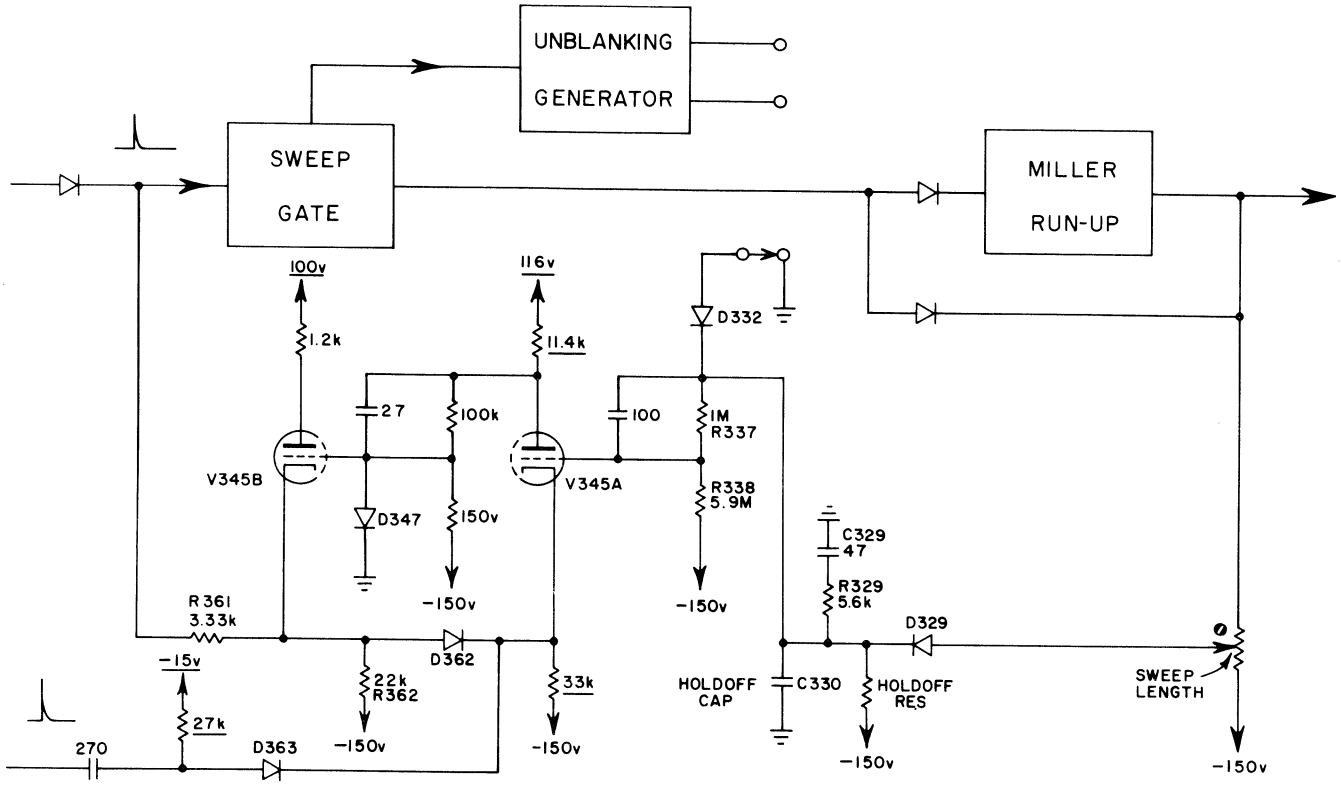
10. The Sweep Length control picks off a portion of the sweep ramp to feed the Hold-Off circuit.

   a. The ramp at the Sweep Length arm runs from -46 to 23v.

   b. R328, C328 overcompensate the Sweep Length divider.

C. Hold-Off Circuit

1. The Hold-Off Multi provides a change of current that flips the Sweep Gating TD to its low state, stopping sweep. It also delays arming the Sweep Gating TD until retrace is finished and the Miller circuit has become stabilized.



TYPE 547 SWEEP GENERATOR A
HOLD OFF MULTI

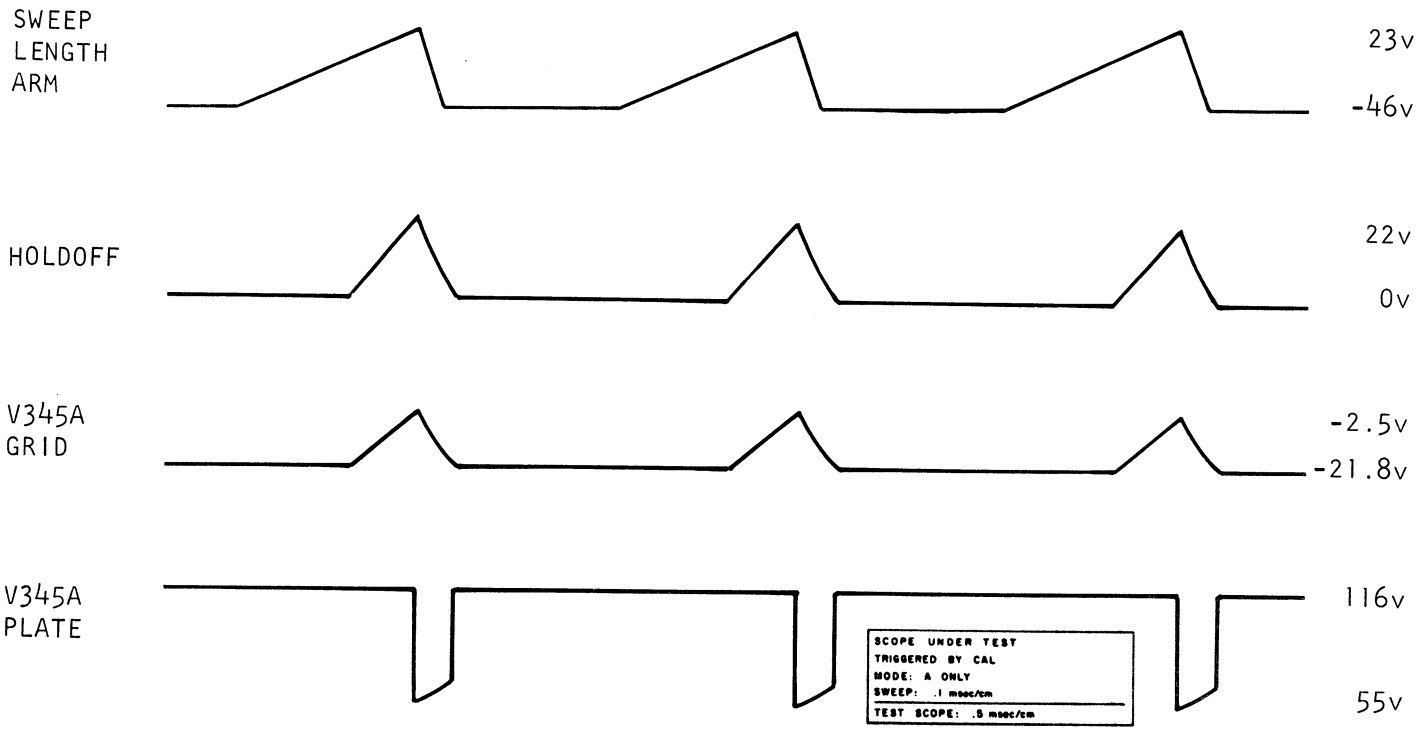
B-547-0013x
4-1-'64 jg

2. The Hold-Off circuit consists of the Hold-Off diode, the Hold-Off resistors and capacitors, and the Hold-Off multi.

3. A dual triode and three diodes are used in the circuit.
   a. V345A and V345B are two halves of a 6DJ8.
   b. D362 is a GE 1N3605 silicon diode.
   c. D332 and D329 are Raytheon 6061 silicon diodes.
4. V345A and V345B form a bistable Schmitt multi.
5. In the quiescent state (the Sweep Gating TD armed awaiting trigger), V345B is conducting and V345A is cut off.
6. Quiescent DC levels V345A, V345B.
   a. V345A grid, -21.8v.
   b. V345A cathode, 1.5v.
   c. V345A plate, 116v.
   d. V345B grid, .6v.
   e. V345B cathode, 1.15v.
   f. V345B plate, 82v.
7. With V345B cathode at 1.5v, .6 ma of the cathode current flows through the Sweep Gating TD.
   a. The .6 ma in addition to the 3.5 ma through R282.
   b. The balance of the cathode current flows through R362 and D362.
8. The Hold-Off Multi remains in its quiescent state until the sweep ramp has reached its required amplitude.
9. The portion of the sweep ramp picked off the SWEEP LENGTH control has a range of -46v to about +23v.
10. The Hold-Off bus is clamped to ground by D332.
    a. The Hold-Off bus cannot go below ground.

b. D329, therefore, is cut off until the sweep waveform on its anode reaches 0v.

c. D332 cuts off and the voltage on the bus raises to 22v charging the Hold-Off capacitor, C330, to this potential.



11. A voltage divider composed of R337 and R338 drops the DC level of the ramp until it has a range of -22v to -2.5v.

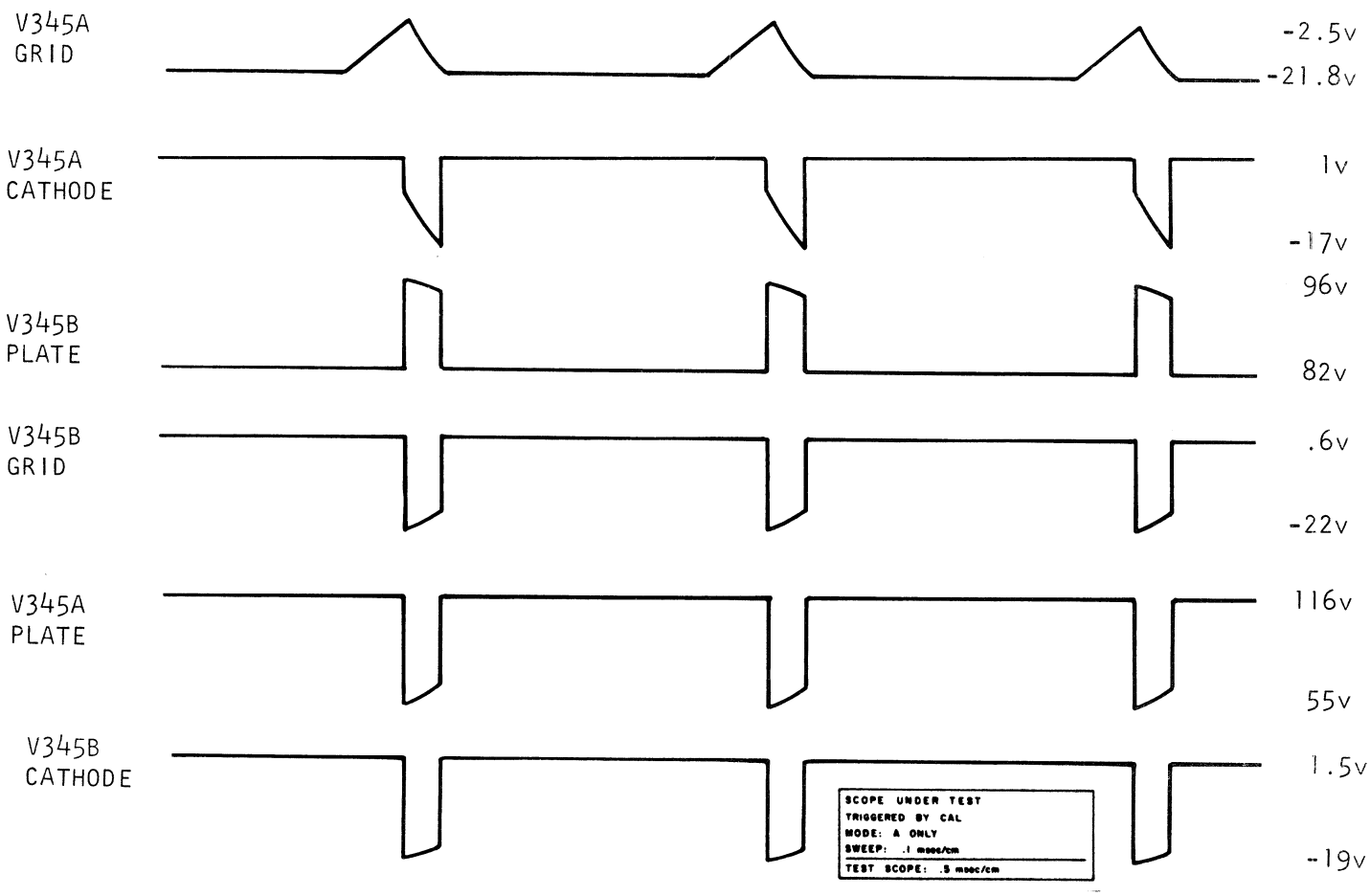
12. V345A cathode is held at 1.5v by current through D362.

a. The plate looks through an equivalent load resistance of 11.4k to 116v.

b. Cut-off bias is -4v.

c. When the grid reaches -2.5v, the tube begins conduction.

13. The multi flips as V345A turns on and V345B turns off.



14. With V345B cut off, its cathode drops to -19v.

    a. D362 cuts off, leaving a divider composed of R361 and R362.

    b. 5.7 ma flows through R361 to the TD circuit.

    c. This current forces 2.2 ma of reverse current through the TD, flipping it to its low state stopping sweep.

    d. The TD is in its locked out condition.

15. V345 plate pulls down to 55v.

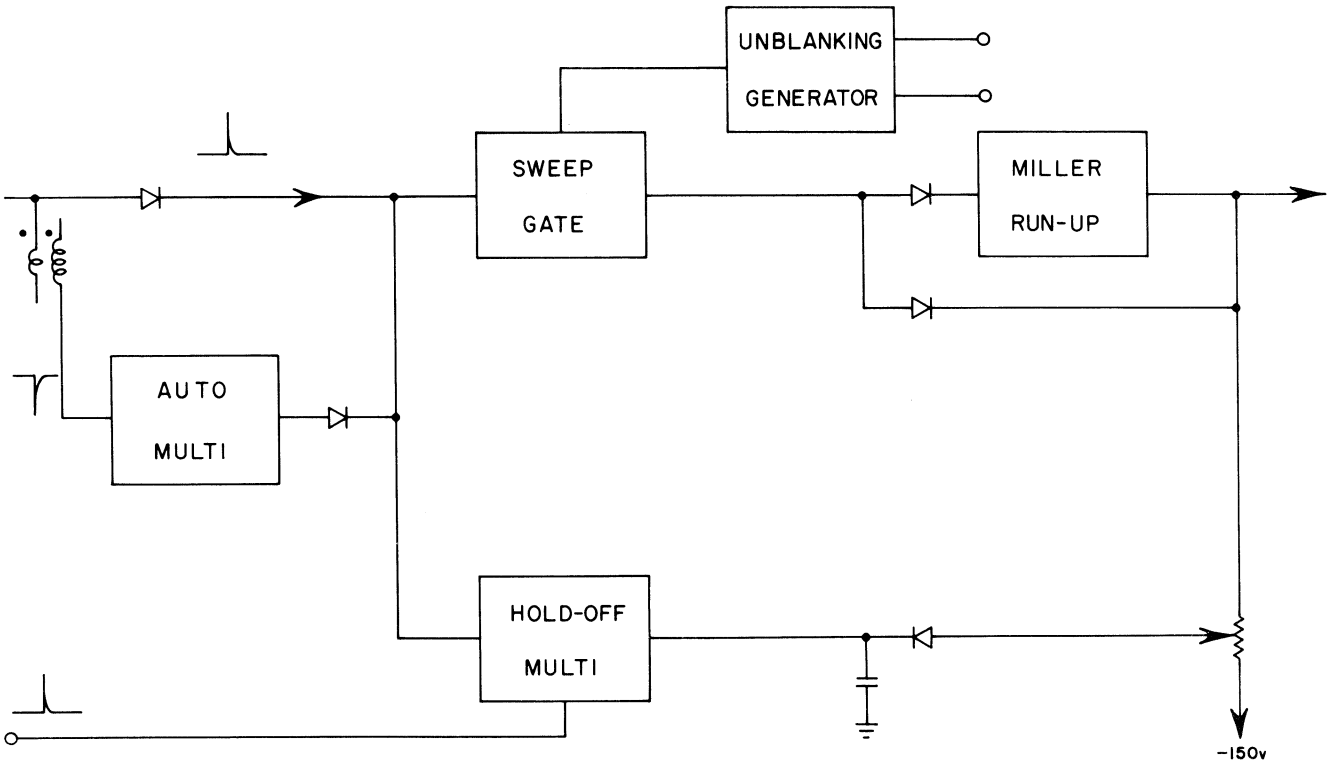
    a. V345B grid drops to -22v as D347 cuts off.

16. As retrace starts and the voltage at the SWEEP LENGTH control starts down, D329, the Hold-Off diode, cuts off.
    a. The Hold-Off capacitor, C330, holds D329 cathode momentarily, allowing the diode to disconnect.
    b. The charge on C330 leaks off slowly through R330, the Hold-Off resistor, providing Hold-Off delay.
        (1) Hold-Off capacitors and Hold-Off resistors are switched with settings of the TIME/CM control.
        (2) On sweep ranges of 5 μsec or faster, C329 becomes the Hold-Off capacitor.
        (3) At the fast sweeps, R329 keeps C329 from delaying the sweep ramp.
17. As the Hold-Off waveform drops V345A grid, its plate rises and its cathode runs down.
18. When V345B grid reaches -20v, its cathode is at -15v, D363 conducts.
19. As V345A grid reaches -22v, D362 conducts.
    a. V345B grid has risen to -22v.
    b. Conducting D362 pulls V345B cathode into conduction.
20. The multi flips.
    a. V345B turns on and V345A cuts off.
    b. The circuit has returned to its quiescent state.

D. AUTO Circuit

1. In the absence of triggers, the AUTO circuit allows the Sweep Circuit to free run at a rate set by the TIME/CM switch.
    a. The feature has been called the "BRIGHT LINE AUTOMATIC".

2. When triggers arrive at a rate of 20 cps or more, the Sweep Circuit is automatically switched to the triggered mode.



TYPE 547 SWEEP GENERATOR A
BLOCK DIAGRAM NO. 2

B-547-0014
4-2-'64 jg

3. The condition when no triggers are present and the AUTO-TRIG switch is in the TRIG mode.

   a. The Sweep Gate TD is armed with 4.1 ma forward current flowing through the diode.

   b. The Hold-Off Multi is in the armed condition -- V345A cut off, V345B conducting.

   c. There is no sweep.

4. The condition when the AUTO-TRIG switch is in the AUTO mode and no triggers are present.

   a. D279 is conducting.

   b. About 1.7 ma flows through the diode.

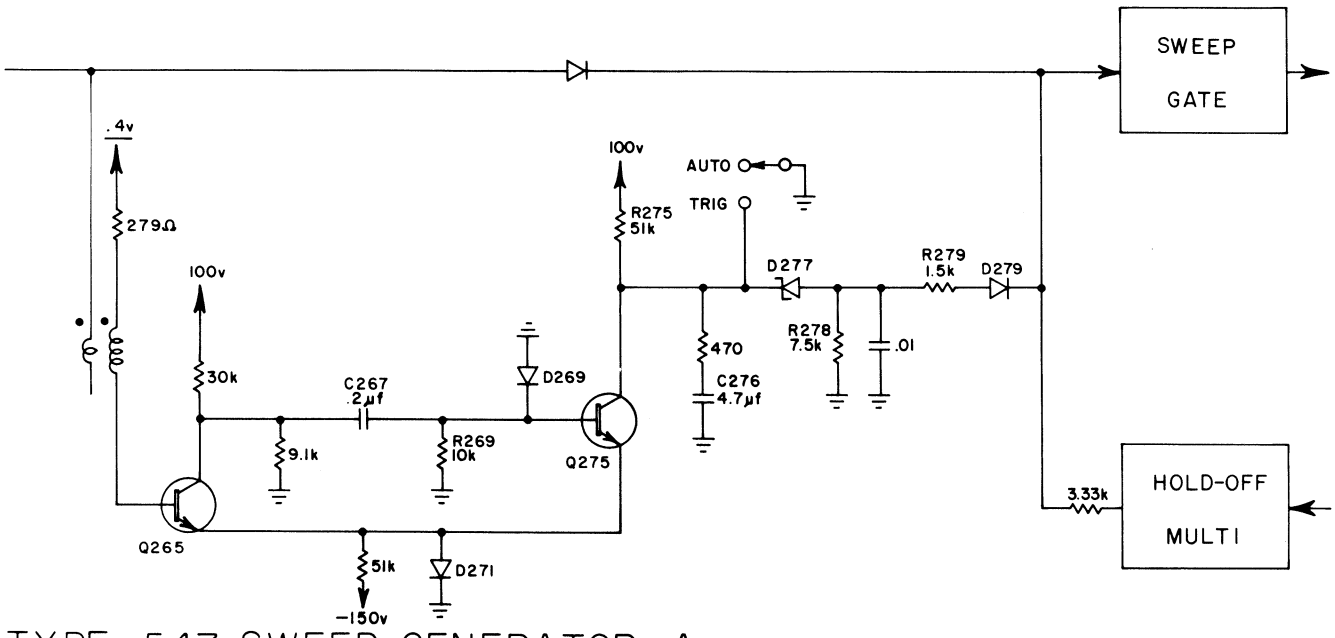
   c. The 1.7 ma comes from the TD.

   d. Added to the quiescent TD current of 4.1 ma, this current will flip the TD to its high state and start sweep.

   e. At the end of sweep when the Hold-Off Multi flips, there is still .8 ma of reverse current available to flip the TD to its low state.

   f. After hold-off, when the Hold-Off Multi returns to its quiescent state, the TD will flip to its high state and begin a new sweep.

   g. The circuit will continue to free run.



TYPE 547 SWEEP GENERATOR A
AUTO MULTI

B-547-0015x
4-7-'64 jg

5. The AUTO Multi is a transistorized monostable multi.
   a. Q265 and Q375 are Motorola 2N2501 silicon NPN transistors.
   b. D271, D269 and D279 are GE 1N3605 silicon diodes.
   c. D277 is a Motorola 1N969A, 10%, 22v zener.
6. In the quiescent condition (no triggers arriving), Q265 is conducting and Q275 is cut off.
   a. Q265 is tied through an equivalent 279Ω to an equivalent .4v.
   b. Q275 base is returned to ground through R269.
7. When the AUTO-TRIG switch is in the AUTO position, a divider is formed of R275, D277 and R278.
   a. D277 anode sets at volts 3v.
   b. 1.4 ma flows through R279 and D279 to keep the sweep free running.
8. When a negative going trigger arrives, Q265 cuts off.
   a. The multi flips to its unstable state.
   b. Q269 is cut off and Q279 is conducting.
   c. Q275 collector pulls down to 1v.
   d. The collector level is dropped by the 22 volt zener to cut off D279.
   e. The AUTO circuit is disconnected from the Sweep Gate.
   f. The Sweep Circuit functions in the normal triggered mode.
9. The Multi remains in its unstable condition for 100 msec.
   a. The Tc is determined by C267 and R269.
   b. While the multi is in the unstable state, C276 charges to 23 volts.

10. When the multi returns to its stable state, C276 begins to charge toward 100v.

    a. If no trigger has arrived by the time C276 has charged to 22 volts, D279 will conduct.

    b. The sweep system will free run.

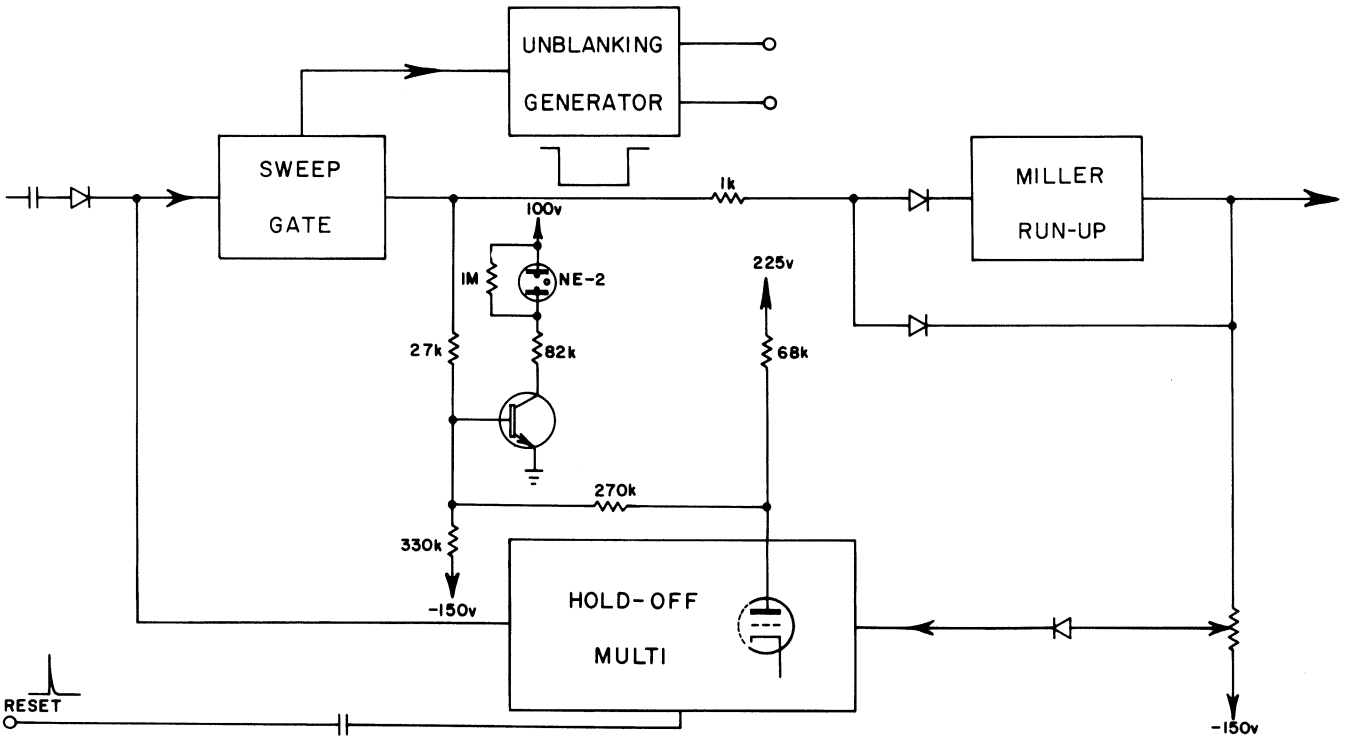
    c. If a trigger arrives within 55 msec, the AUTO Multi will recycle.

    d. C276 will not charge high enough to allow D279 to conduct.

    e. As long as D279 remains cut off, the sweep will not free run.

E. Ready Light Circuit

1. The Ready Light indicates when the sweep circuit is ready to accept a trigger.



TYPE 547 SWEEP GENERATOR A
READY LIGHT INDICATOR

B-547-0016x
4-9-'64 jg

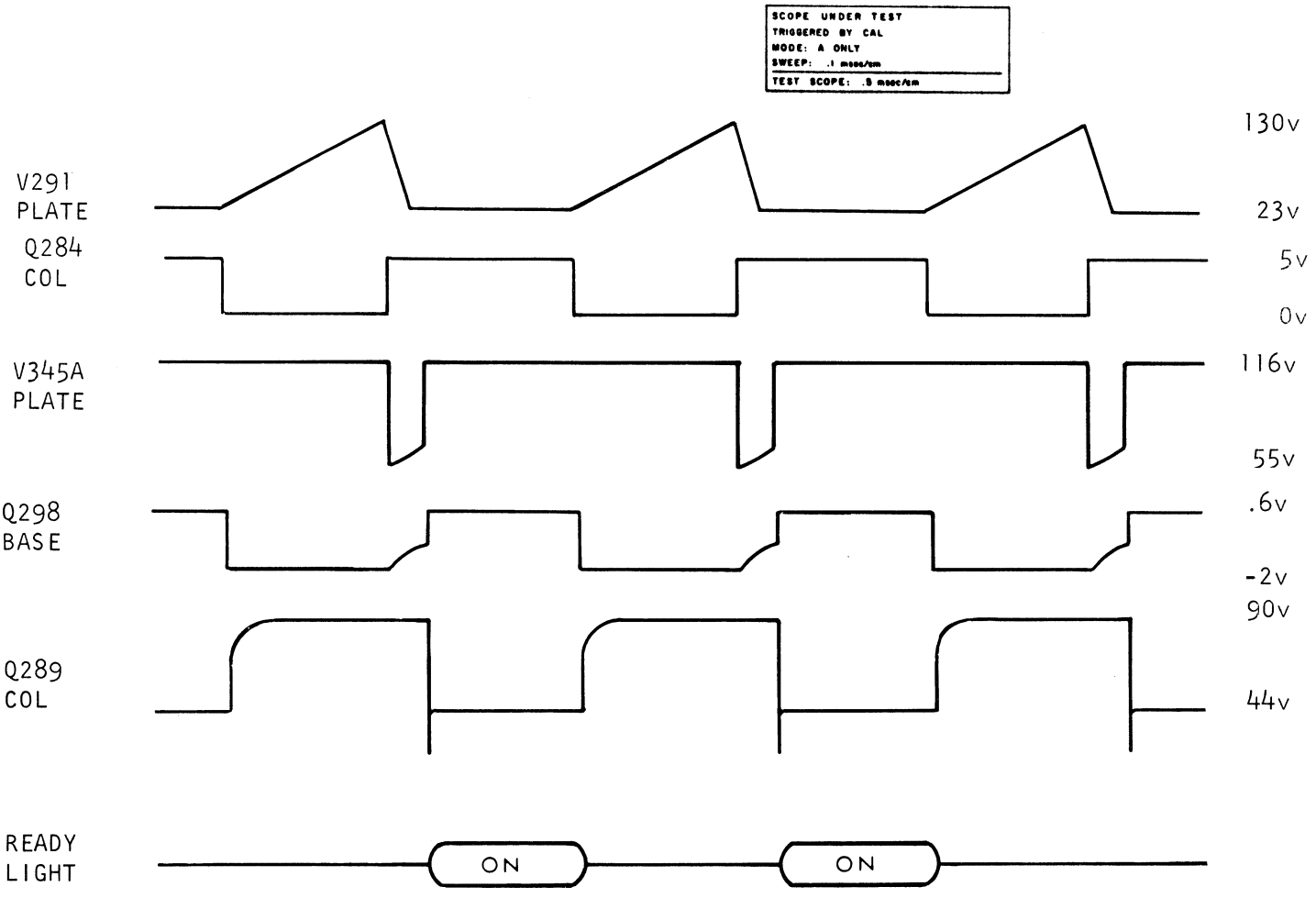
a. The Ready Light neon (B-289) lights when the Sweep Gating TD is in its low state and the Hold-Off Multi is in its quiescent state (V345A cut off).

b. It extinguishes as soon as sweep starts.

2. The circuit uses a transistor and a neon.

a. Q289 is a 2N1893 silicon NPN transistor.

b. B289 is a NE2 neon.



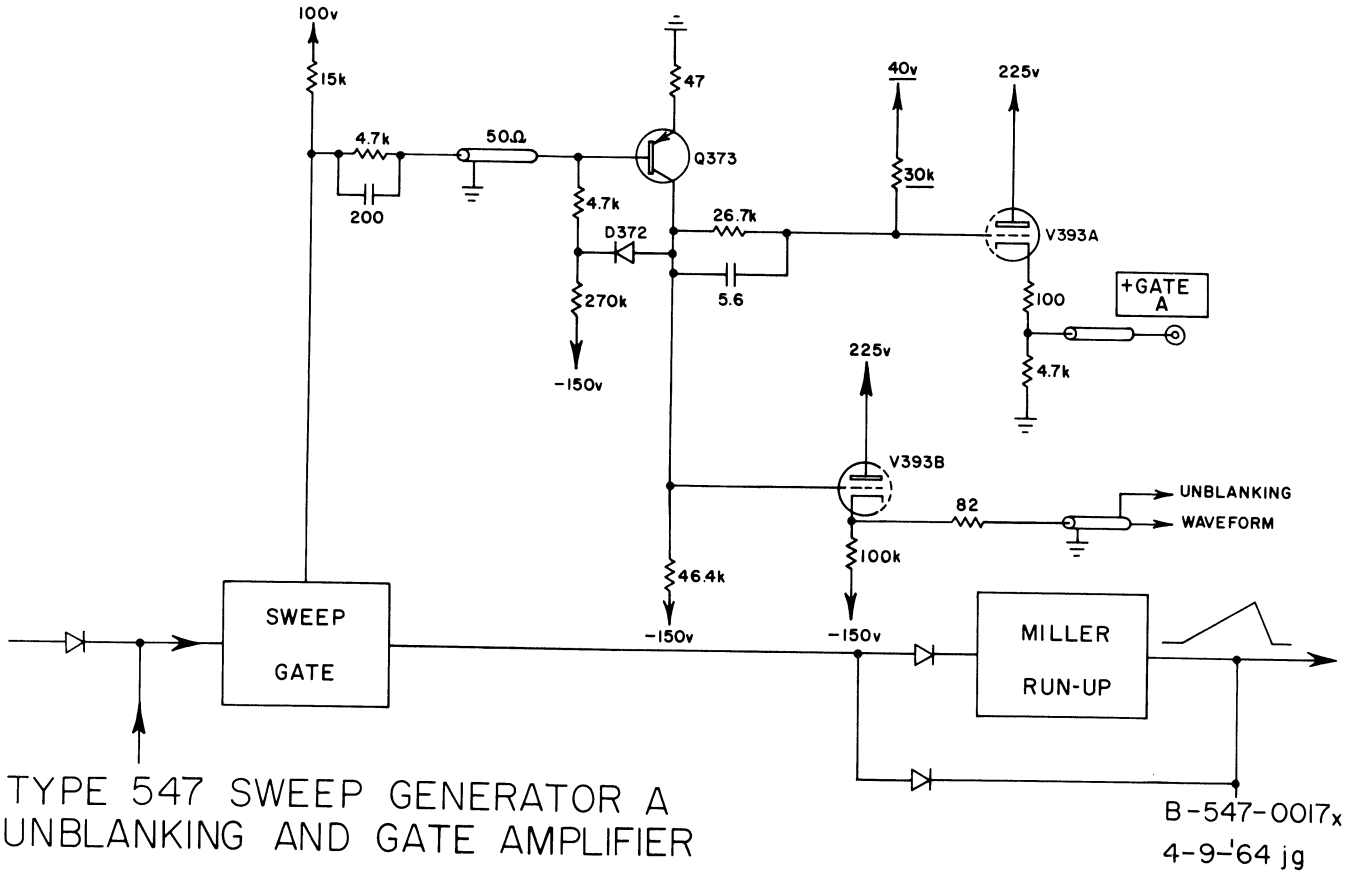
3. The Ready Light driver transistor (Q289) will conduct only when V345A in the Hold-Off Multi is cut off.
   a. The circuit can be considered an AND gate.
   b. When V345A is cut off and Q289 collector is at 5.4v, the Ready Light lights.
4. When a trigger arrives, the TD flips into its high state, biasing Q284 into saturation.
   a. Sweep starts.
   b. Q284 collector drops to near ground.
   c. Q289 base comes down.
   d. Q289 collector rises.
   e. The Ready Light is extinguished.
5. At the end of sweep, the Hold-Off Multi flips, bringing V345A into conduction.
   a. Q289 base is pulled down to cut off.
   b. The TD goes into its reverse biase condition.
   c. Q284 collector goes up.
   d. Q289 base is pulled up, but not far enough for conduction.
6. At the end of hold-off, the Hold-Off Multi flips back, cutting off V345A.
   a. V345A plate rises to 116v, bringing the Q289 into conduction.
   b. The TD goes to its quiescent state (awaiting a trigger).
   c. The Ready Light neon lights.

F. Unblanking and Gate Amplifier

1. The circuit provides a positive going unblanking waveform and a + Gate waveform with the same duration as the Sweep.

   a. The unblanking waveform is 60v peak-to-peak.

   b. The GATE A waveform has an amplitude of 25v peak-to-peak.



TYPE 547 SWEEP GENERATOR A
UNBLANKING AND GATE AMPLIFIER

B-547-0017x
4-9-'64 jg

2. V393A and V393B are each one-half 6DJ8.

3. Q373 is an Amperex 2N2207 (PADT-35) germanium PNP transistor.

4. D372 is a Raytheon 6061 silicon diode.

5. The condition prior to sweep.
   a. Q284 collector, 5.4v.
   b. Q373 base, 1.6v.
   c. Q373 collector, -64v.
   d. V373B cathode, -54v.
   e. V393A grid, 015v.
   f. V393A cathode, 0v.
6. Condition during sweep.
   a. Q284 collector, 0v.
   b. Q373 base, -.4v.
   c. Q373 collector, -1v.
   d. V393B cathode, 7v.
   e. V393A grid, 19v.
   f. V393A cathode, 25v.
7. Prior to sweep, Q373 is cut off.
   a. A voltage divider composed of R374 and R376, R390 sets the collector at -64v.
   b. D372 is cut off.
8. V393A is cut off with its grid at -15v and the cathode at ground.
9. V393B is conducting.
   a. The grid is at -64v.
   b. With about 1 ma flowing, the CF has 10v bias.
   c. The cathode sets at -54v.

10. Sequence of operation as sweep begins.

    a. As Q284 saturates, its collector drops to 0v.

    b. Q373 base drops to -.4v biasing the transistor to heavy conduction.

    c. Q273 is held short of saturation by the feedback loop as D273 conducts.

    d. With Q273 conducting, new levels are set at V393A and V393B grids.

        (1) V393A grid raises to 19v.

        (2) V393B grid raises to 0v.

    e. As V393A cathode raises to 25v, the Gate waveform is formed.

        (1) Output impedance is about 250Ω.

    f. V393B cathode raises to 7v forming the 60v unblanking waveform.

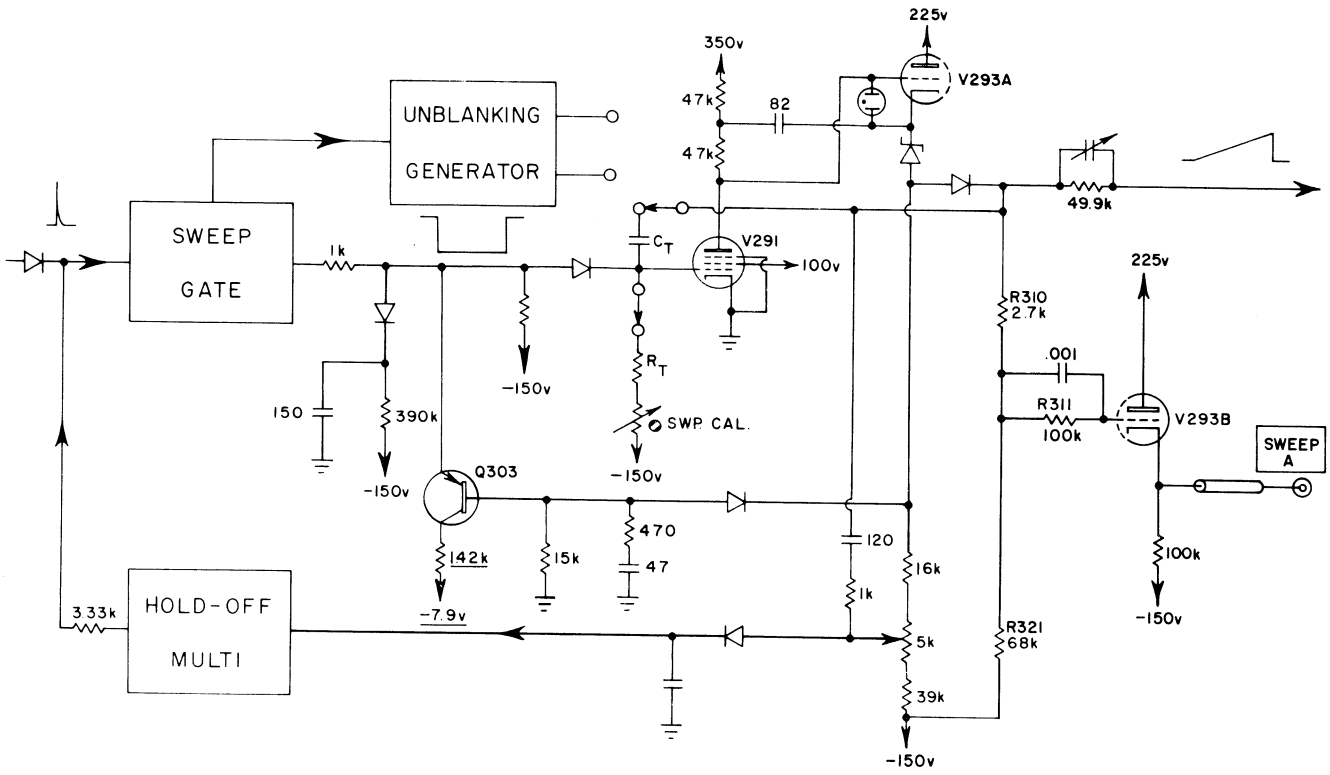
G. SWEEP A Output CF

1. The SWEEP A Output CF supplies a 100v sweep ramp to a front panel jack.

2. V293B is the other half of the 6DJ8 used in the Run-Up CF circuit.

3. Output impedance is about 100Ω

    a. A load of less than 10k will exceed 6DJ8 plate dissipation.



TYPE 547 SWEEP GENERATOR A
SWEEP A OUTPUT

B-547-0018x
4-10-'64 jg

4. The divider composed of R310 and R321 places the start of the ramp at 0v.

5. R311 offers some protection should the output jack become momentarily shorted to ground -- a direct short will blow the tube.

   a. A short to ground will shorten sweep and affect timing at sweep speeds above 1 μsec/cm.

H. SINGLE SWEEP

1. Single Sweep mode is selected by a front panel level wafer switch.

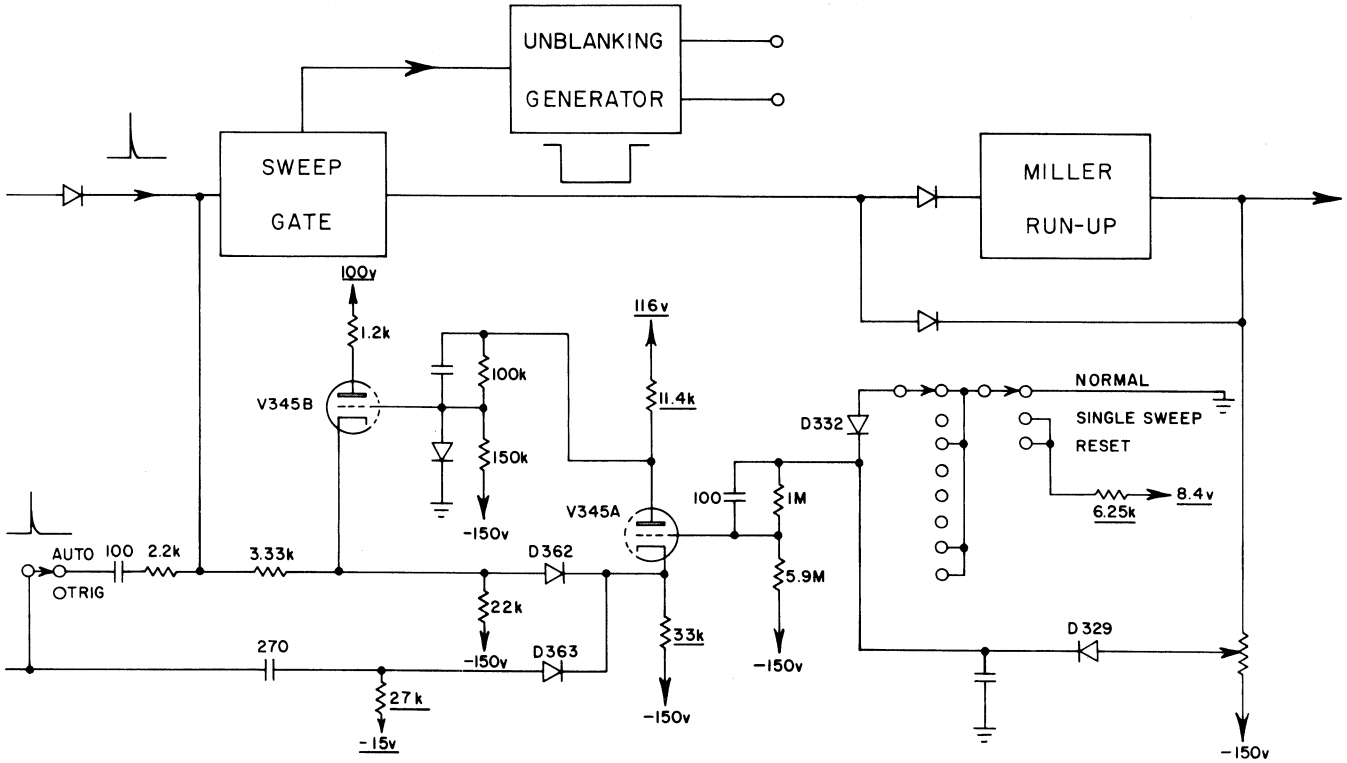
   a. Three positions: NORMAL, SINGLE SWEEP, and RESET.

2. Three modes of SINGLE SWEEP operation are available.

   a. Manual RESET in the AUTO mode.

   b. Manual RESET in the TRIG mode.

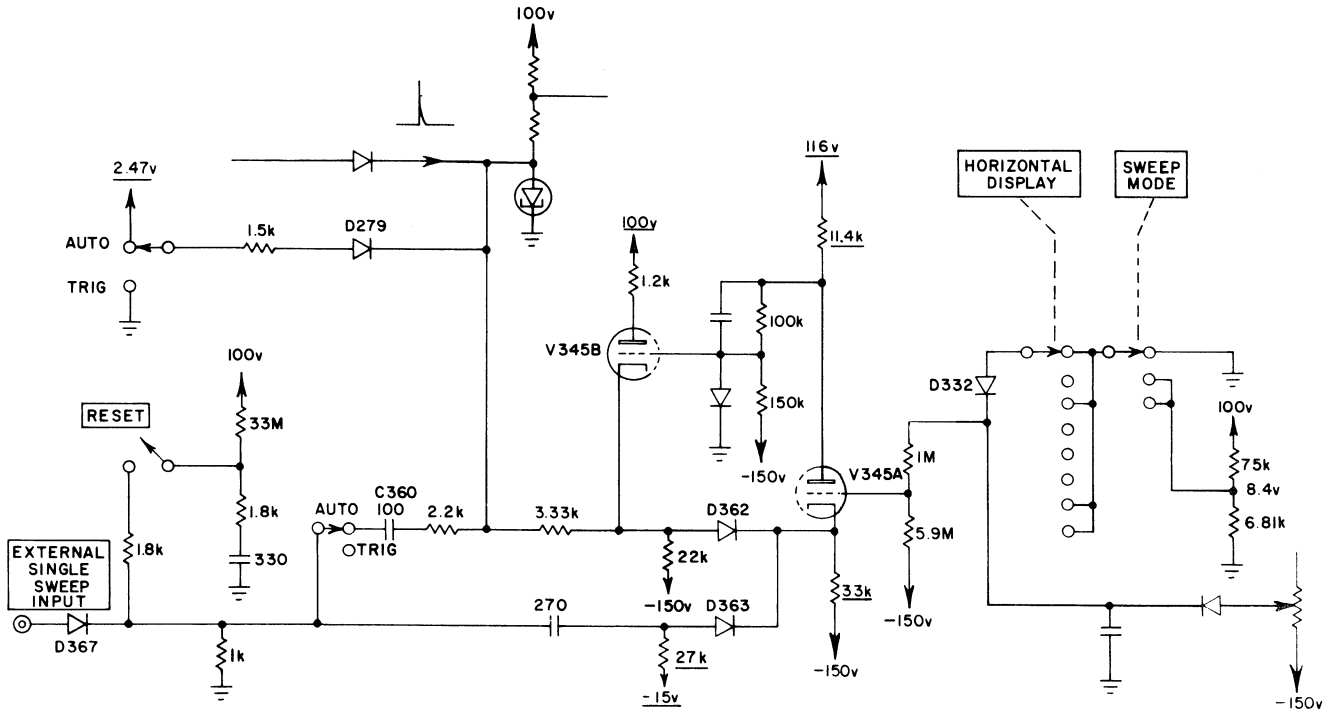
   c. EXTERNAL SINGLE SWEEP mode.



TYPE 547 SWEEP GENERATOR A
SINGLE SWEEP NO.1

B-547-0019x
4-10-'64 jg

3. The SINGLE SWEEP function of the sweep circuit utilizes the operation of the Hold-Off Multi.



TYPE 547 SWEEP GENERATOR A
SINGLE SWEEP NO.2

B-547-0020x
4-14-'64 jg

4. Switching the SINGLE SWEEP mode switch to SINGLE SWEEP places the Hold-Off Multi in its "locked out" condition.

   a. D332 ties to an equivalent of 6.25k to 8.4v.

   b. V345A grid is lifted by D332 to -15.5v.

   c. V345A conducts, V345B is cut off.

   d. V345A cathode is at -14v.

   e. D362 and D363 are cut off.

5. SINGLE SWEEP condition in the AUTO mode.
   a. D279 is conducting.
   b. When the Hold-Off Multi flips sweep will start without waiting for a trigger.
6. When the SINGLE SWEEP switch is pressed to RESET (spring return to SINGLE SWEEP), a 20v positive going pulse is generated.
   a. The pulse turns on D363.
   b. V345A cathode is lifted out of conduction.
   c. The Multi flips (V345B conducting, V345A cut off).
   d. The Sweep Gating TD flips to its high state and sweep starts.
   e. The pulse also couples through C360 to flip the TD about 100 nsec before the Hold-Off multi completes its transition.
      (1) This premature flipping of the TD is incidental to this mode, but is essential to Delayed Sweep operation.
7. At the end of Sweep, the Hold-Off Multi will flip as in normal operation.
8. As the Hold-Off waveform drops V345A grid, D332 conducts.
   a. Hold-off cannot be completed.
   b. V345A stays in conduction.
   c. The circuit remains in the locked out condition.
   d. The circuit has delivered a single sweep.
9. SINGLE SWEEP condition in the TRIG mode.
   a. D279 is cut off.
   b. When the Hold-Off Multi flips, the Sweep Gating TD is armed and will flip to its high state with the arrival of the first trigger.

10. Like in AUTO mode operation, the RESET pulse lifts V345A cathode to cut-off and flips the Hold-Off Multi.
    a. The Sweep Gating TD has 4.1 ma forward current flowing.
    b. The TD is in its armed state.
    c. The READY LIGHT lights.
    d. Arrival of the first trigger will flip the multi and start sweep.
11. At tne end of sweep, the Hold-Off Multi will flip, stopping sweep as in normal operation.
    a. The READY LIGHT goes out.
12. Hold-off cannot be completed, however, as the hold-off bus is clamped by D332 to +8.4v.
13. The circuit is locked out at the end of a single sweep and will not respond to a trigger.
14. Another RESET pulse will rearm the circuit.
15. An EXTERNAL SINGLE SWEEP jack (BNC) is available on the scope rear panel.
    a. A positive going 20v reset pulse may be used to RESET the sweep circuit.
    b. .5 μsec risetime or better is required.
16. D367 disconnects if the RESET switch is actuated when the EXT SINGLE SWEEP INPUT is in use.
    a. This prevents a kickback out the EXT jack.

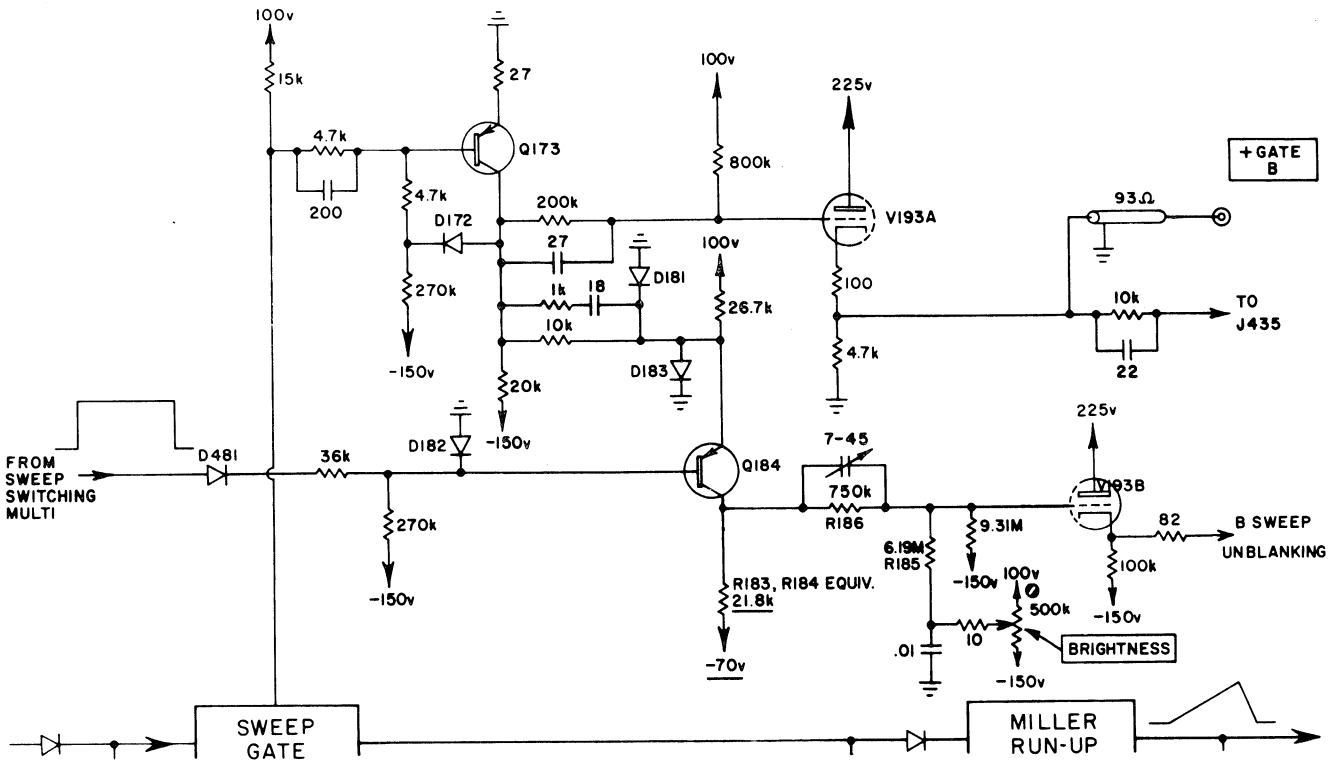
TYPE 547

V. B SWEEP GENERATOR

A. The B Sweep Generator has the same sweep speeds and the same general circuitry as the A Sweep Generator.

1. No SWEEP OUT waveform available.
2. The unblanking circuit has additional provisions for B Sweep intensification lockout and intensification BRIGHTNESS.
3. Lockout circuits are provided that are explained in the section, Horizontal Display modes.
4. The B Sweep ramp feeds the Delay Pickoff circuit.

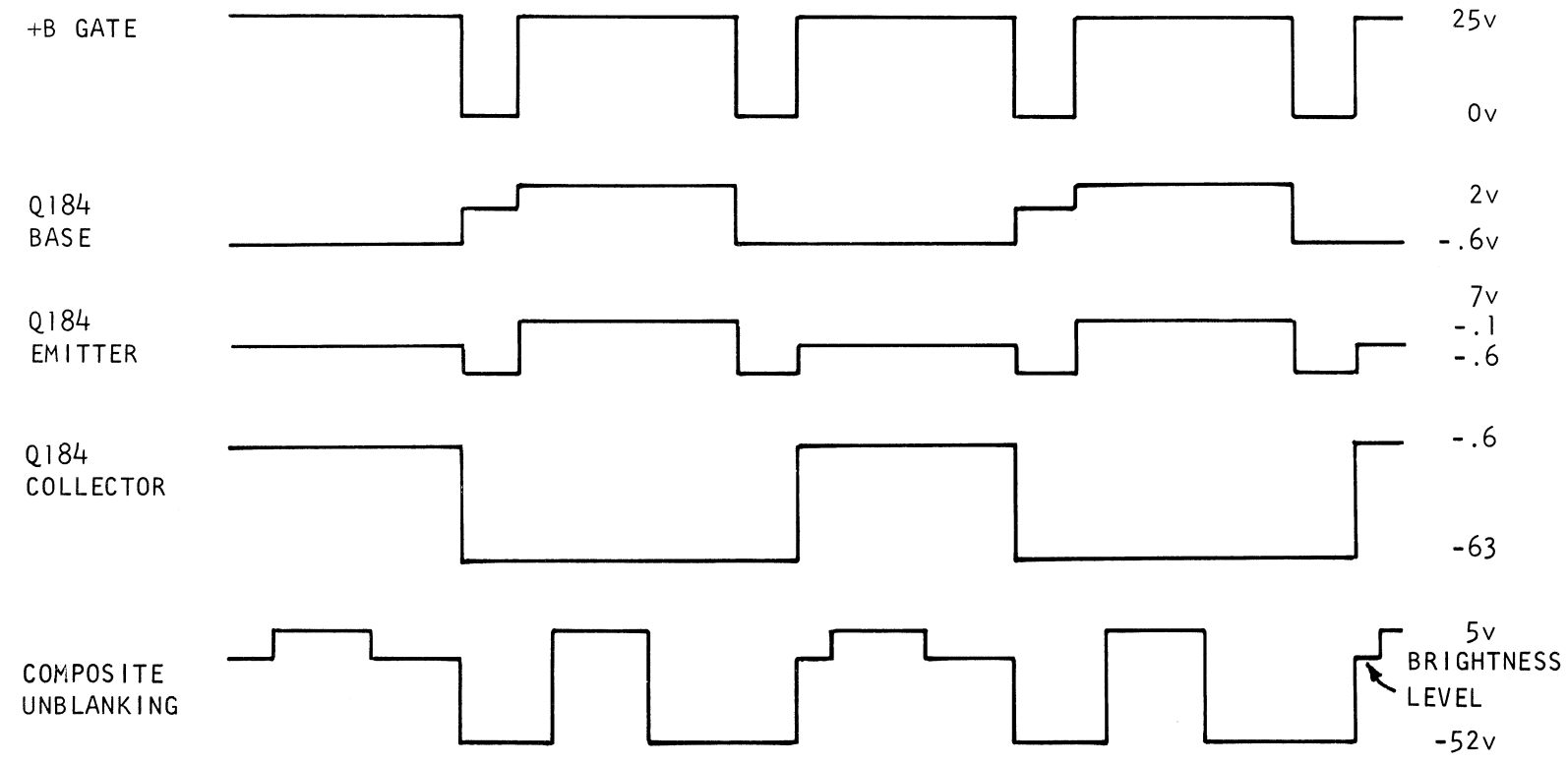
B. Unblanking Amplifier



TYPE 547 SWEEP GENERATOR B
UNBLANKING AND GATE AMPLIFIER

B-547-002lx
4-15-'64 jg

1. The + GATE B circuit is the same as the GATE A circuit.
   a. The B GATE delivers a 25v positive going gate whenever the B Sweep is in operation.
2. The Unblanking circuit contains a logic gate that functions in both ALT modes -- it is needed, however, only when A DLY'D BY B in the DLY'D ALT mode.
   a. In these modes the gate prevents B unblanking from being developed while the A Sweep is being displayed.
   b. A lockout waveform from the Sweep Switching circuit provides the gate that turns off B unblanking.
   c. In the DLY'D ALT mode the logic gate turns off B unblanking while A DLY'D BY B is being displayed.
   d. The circuit allows B unblanking to be mixed with A unblanking while B INTENS BY A is being displayed.



3. In the normal operation (B unblanking not gated off), Q184 emitter swings from a quiescent -.6v, limited by D181, to about 0v during sweep.
   a. Q184 base is clamped by D182 at -.6v.
   b. Q174 collector swings from about -49v to -.5v during sweep.
4. Prior to sweep, Q184 is cut off.
   a. The collector sets at -63v.
      (1) R183, R184 is equivalent 21.8k collector load resistance to -70v.
   b. V193B cathode is at -50v.
5. During sweep, Q184 emitter pulls up to about -.2v.
   a. The transistor saturates.
   b. The collector pulls up to -.6v.
   c. V193B cathode raises to +9v.
6. In the ALT modes, while A Sweep is being displayed, a 27v waveform from the Sweep Switching Multi cuts off D182 and pulls up on Q184 base.
   a. Q184 cuts off.
   b. Prior to the start of B Sweep (in A DLY'D BY B mode), Q184 emitter is held at -.6v by Q173 collector (limited by D181).
   c. Q184 base is held at about 1v by base-emitter breakdown.
   d. At the start of B Sweep, the B gate raises Q184 emitter to be limited by D183 at .6v.

e. Q184 base raises (still limited by base emitter breakdown) to about 1.2v.

(1) R181 limits breakdown current.

f. Q184 remains cut off; the B unblanking circuit is locked out.

7. At the end of the lockout waveform, Q184 base drops to -.6v (clamped by D182).

a. Q184 can again function as the unblanking amplifier.

8. R186 and R185 allow mixing of unblanking and brightness information.

9. The Brightness adjust varies the top of the B Unblanking waveform from +4v to -17v.

a. The Brightness adjust is a front panel fingertip adjustment.

b. The control sets B Sweep brightness in all modes although the control is designed to adjust brightness contrast in B INTENS BY A mode and to normalize brightness in the ALT mode with widely different sweep speeds or duty factor.

10. V193B grid swings from -60v* to 10v at a nominal Brightness adjust setting.

11. V193B cathode swings from -52v to 5v.

12. The output goes by coax to the Unblanking mixer in the CRT circuit.

* Measurements loaded with 10M probe impedance.

VI. HORIZONTAL DISPLAY MODES

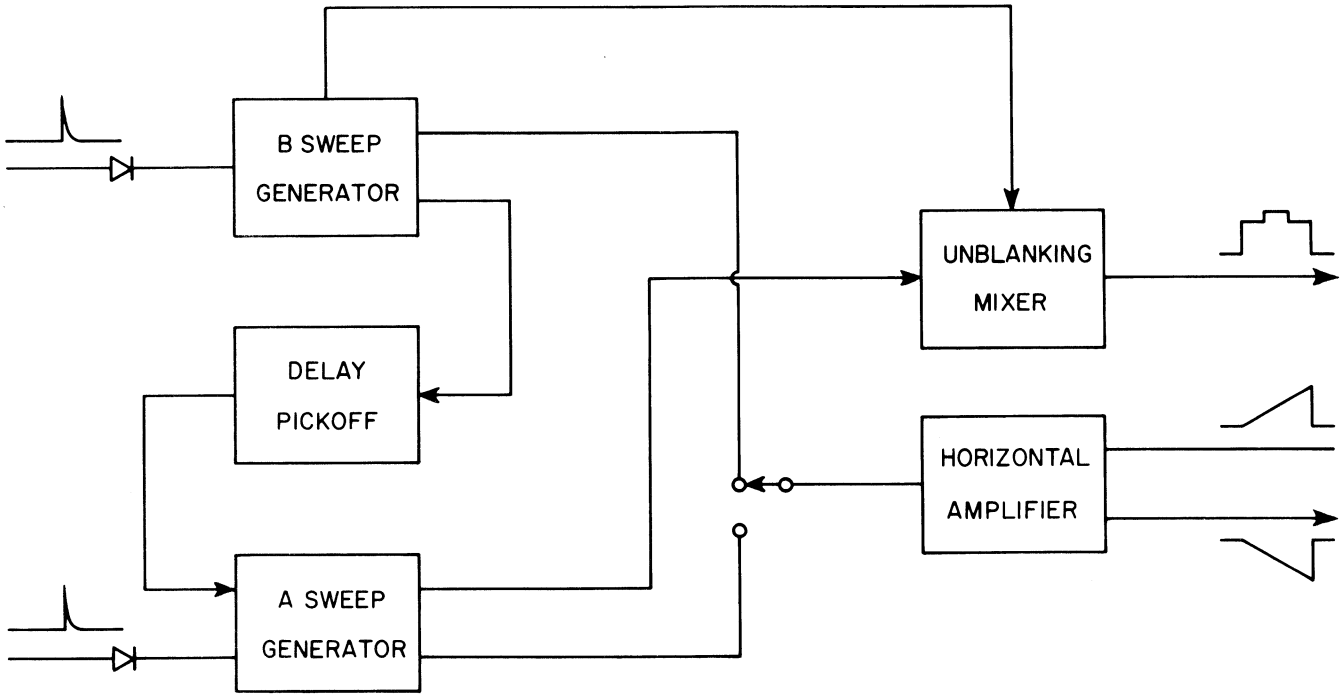
A. Seven Display modes are available.

1. A - Only A Sweep is displayed.
2. B - Only B Sweep is displayed.
3. A ALT B - Both A and B Sweeps are displayed alternately.
4. B INTENS BY A - The B Sweep is displayed, but the A Sweep intensifies a portion of the display.
   a. In this mode, an anti-wrap-around feature prevents A Sweep from running beyond the end of B Sweep.
5. A DLY'D BY B - The A Sweep is displayed, having been delayed a calibrated time interval by B Sweep.
6. B INTEN - ALT - A DLY'D - The INTENS and DLY'D modes are displayed alternately.
7. EXT HORIZONTAL INPUT.

B. B INTEN BY A Mode

1. Initially, only the B sweep can accept a trigger -- A Sweep is locked out.

a. B Sweep is displayed.



TYPE 547 HORIZONTAL DISPLAY MODES
B INTENSIFIED BY A, BLOCK DIAGRAM

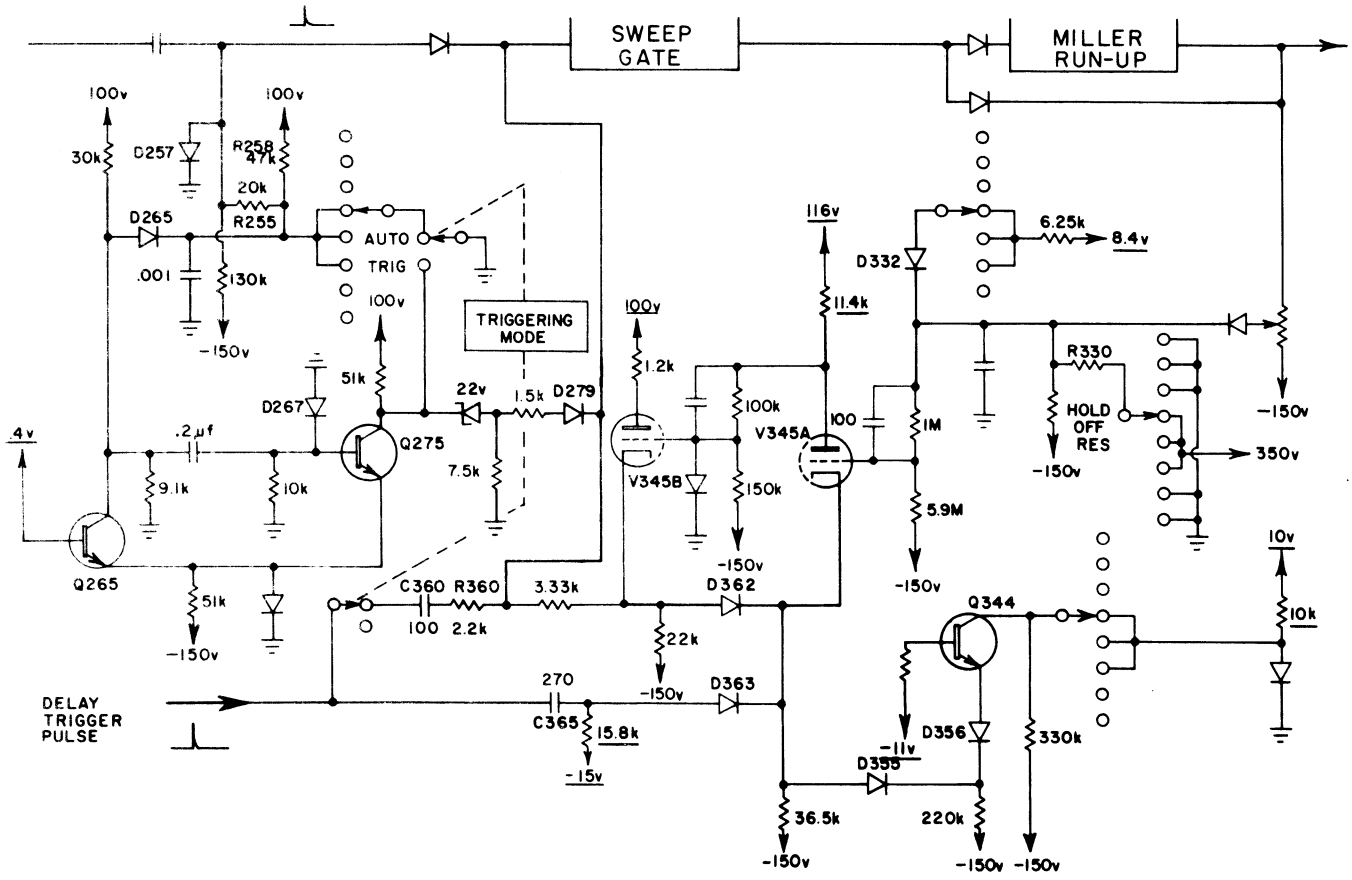
B-547-0082
4-22-'64 ms

2. As B Sweep begins to run up, a trigger arrives from the Delay Pickoff circuit.

   a. A Sweep begins to run up.

3. A composite of the two sweeps is displayed; the A Sweep intensifying the B Sweep display.

4. A Sweep quiescent condition in AUTO mode.



TYPE 547 HORIZONTAL DISPLAY MODES
B INTENSIFIED BY A, A SWEEP

B-547-0077
4-22-'64 jg

a. R255 connects to ground instead of to +100v through R258.

(1) D259 anode pulls down to -20v cutting off the diode.

(2) No triggers can reach the Sweep Gating TD.

b. D265 clamps Q265 collector to ground disabling the Auto Multi.

(1) D279 is conducting 1.5 ma from the Sweep Gating TD.

c. D332 anode ties through an equivalent 6.25k to 8.4v.

(1) Hold-off cannot flip the Hold-Off Multi to its armed state.

(2) The Hold-Off Multi is flipped by a delayed trigger from the Delay Pickoff circuit.

d. R330 in the hold-off circuit returns to +350v instead of ground.*

(1) Extends hold-off time.

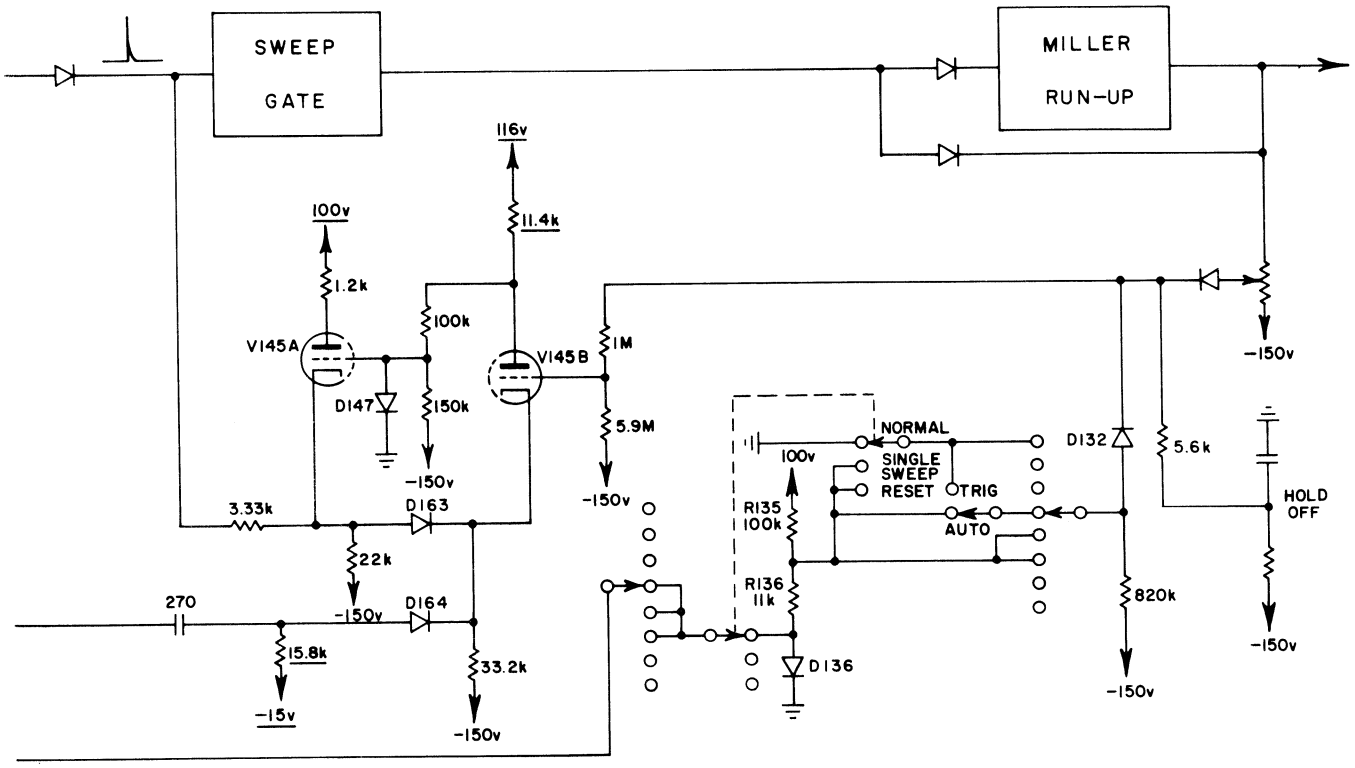
e. Q344 collector ties to a diode in the B Sweep Generator which clamps it to .6v.

f. An output from the Delay Pickoff is connected to C360 and C365.

g. Single Sweep circuit is disabled.

* See A Sweep Timing Switch.

5. B Sweep quiescent condition in AUTO mode.



TYPE 547 HORIZONTAL DISPLAY MODES
B INTENSIFIED BY A, B SWEEP

B-547-0078x
4-23-'64 jg

a. The Auto circuit is functioning.

(1) In the absence of triggers, B Sweep will free run.

(2) With triggers, the circuit will trigger normally.

b. D132 anode is tied through the Horizontal Display switch and the A Sweep AUTO switch to 10v.

(1) Divider R135, R136 is equivalent 10k to 10v.

(2) Hold-off cannot flip the multi to its ready state.

(3) D136 clamps the bottom of the divider to ground.

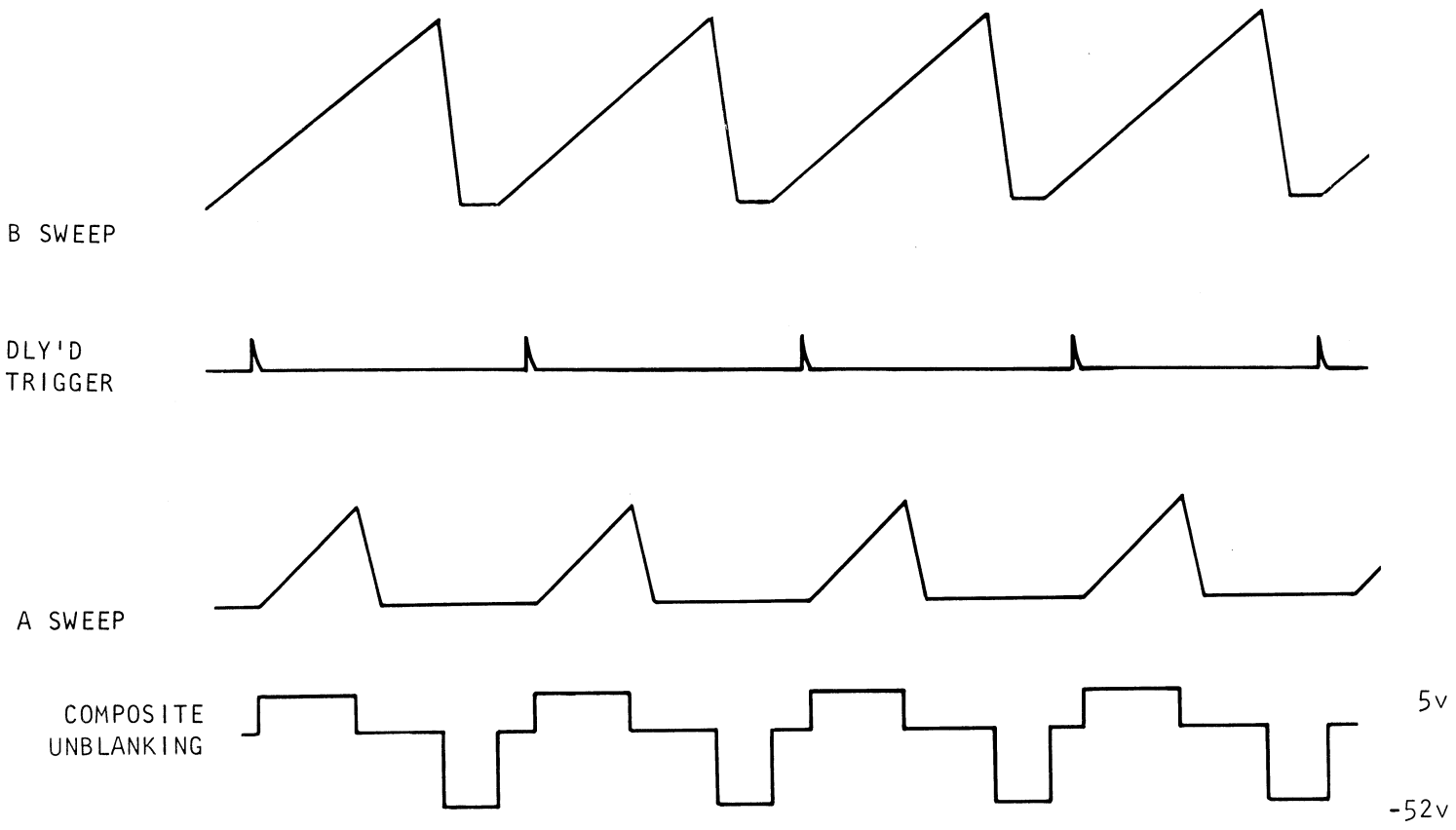
(4) At the end of A Sweep, the bottom of the divider drops to -11v.

(5) D132 anode pulls down to ground.

(6) B hold-off can be completed.

(7) The B Hold-Off Multi can switch to the ready state.

c. The B Sweep ramp is fed to the Delay Pickoff.



6. Operation in the AUTO mode at start of Sweep.

   a. AUTO mode in this instance has a different function than AUTO triggering.

      (1) In this mode, the A Sweep will start as soon as armed by the Delay Trigger.

      (2) The Auto Multi is disabled.

   b. B Sweep begins to run up.

   c. The B Sweep ramp is fed to the Delay Pickoff.

   d. At a time delay determined by the B Sweep timing and the DELAY TIME MULTIPLIER, a positive going Delayed Trigger arrives at the A Sweep Generator.

   e. Coupled through C360, R360, the Delay Trigger pulls a 6 ma current pulse out of the A Sweep Gating TD.

      (1) This current pulse plus the 1.5 ma flowing through D279 is enough to overcome the 2.2 ma reverse current through the TD and flip it to its high state to start sweep.

   f. The same Delayed Trigger lifts D363 into conduction.

   g. V345A cathode current is diverted through D363.

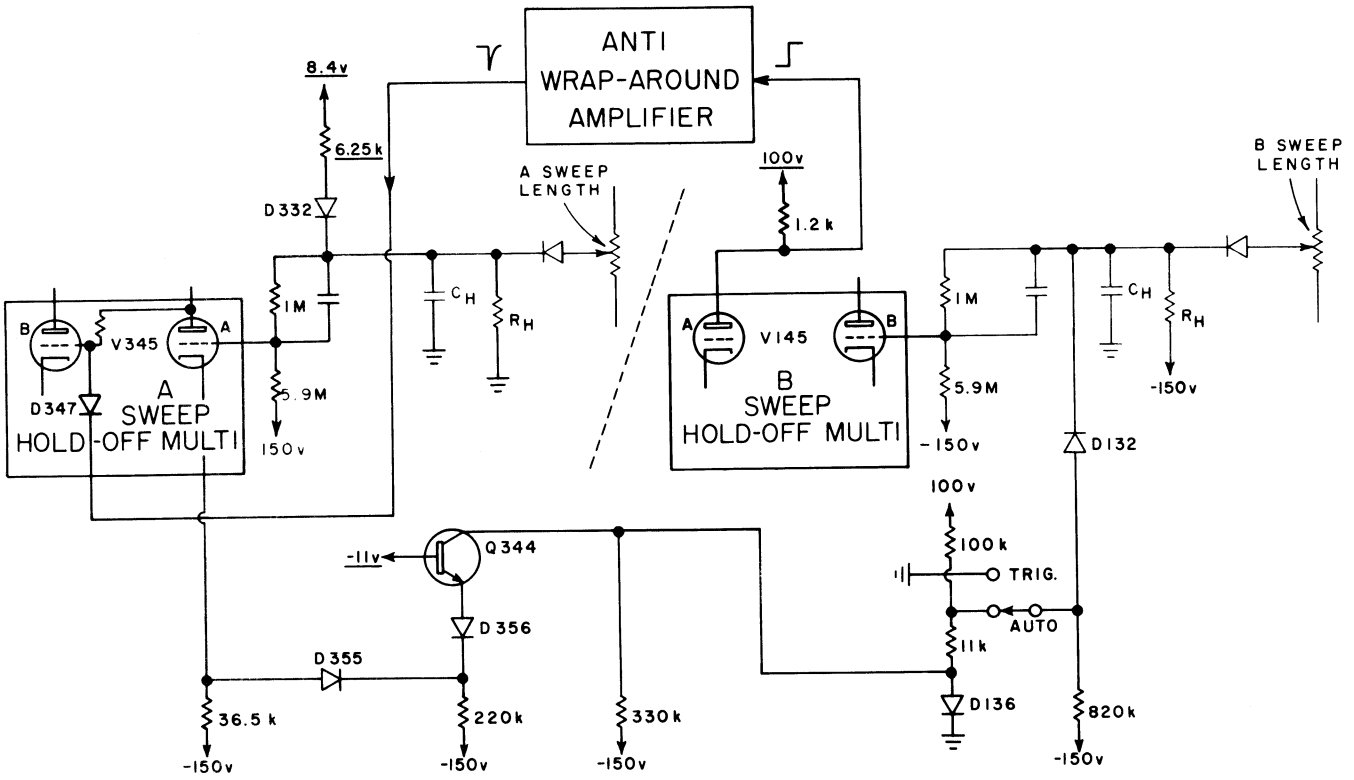
   h. V345A cuts off and the Hold-Off Multi flips.

      (1) Sweep has already started 100 nsec earlier.

      (2) The Multi is now in the position to hold the Sweep Gating TD in its high state until the end of sweep.

i. As sweep starts, the A Sweep unblanking waveform adds to B sweep unblanking to intensify the portion of the B display that represents A Sweep duration.

7. Operation in the AUTO mode at the end of sweep.



TYPE 547 HORIZONTAL DISPLAY MODES
B INTEN. BY A, LOCK OUT CIRCUITS (AUTO MODE)

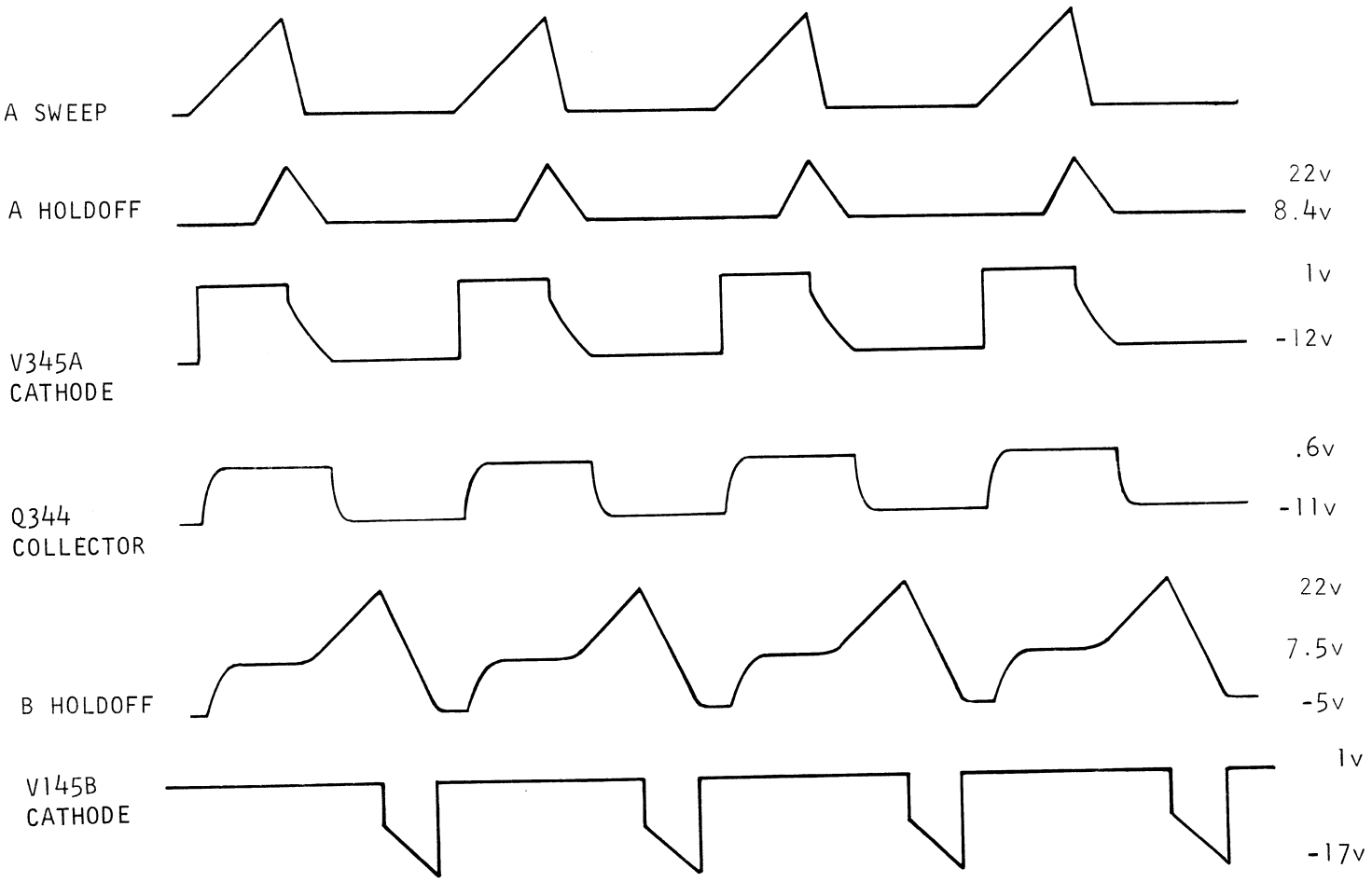
B-547-0079x
4-23-'64 ms

a. If A Sweep terminates before B, the A Sweep Hold-Off Multi switches in the normal manner and hold-off starts.

(1) Hold-off is not completed as D332 clamps the hold-off bus at 8.4v.

(2) The A Hold-Off Multi remains in its locked out mode.

b. As A Sweep Hold-Off Bus reaches its 8.4v lockout point, V345A cathode will have dropped to -12v.



c. As V345A reaches -12v, D355 cuts off and D356 turns on.

d. Current through D356 pulls Q344 into saturation.

(1) Q344 base sets at -11v.

(2) Q344 collector pulls down to -11v.

(3) D136 (B Sweep Diagram) disconnects.

(4) D132 anode pulls down to 0v.

(5) At the end of B Sweep, B hold-off can be completed.

e. As B Sweep is completed, the B Hold-Off Multi switches in the normal manner and hold-off starts.

(1) With D132 anode at 0v, B hold-off can be completed.

(2) At the end of B hold-ff, the B Hold-Off Multi flips to its ready state.

(3) The next trigger will start sweep again.

f. If A Sweep is set to run longer than the end of B Sweep:

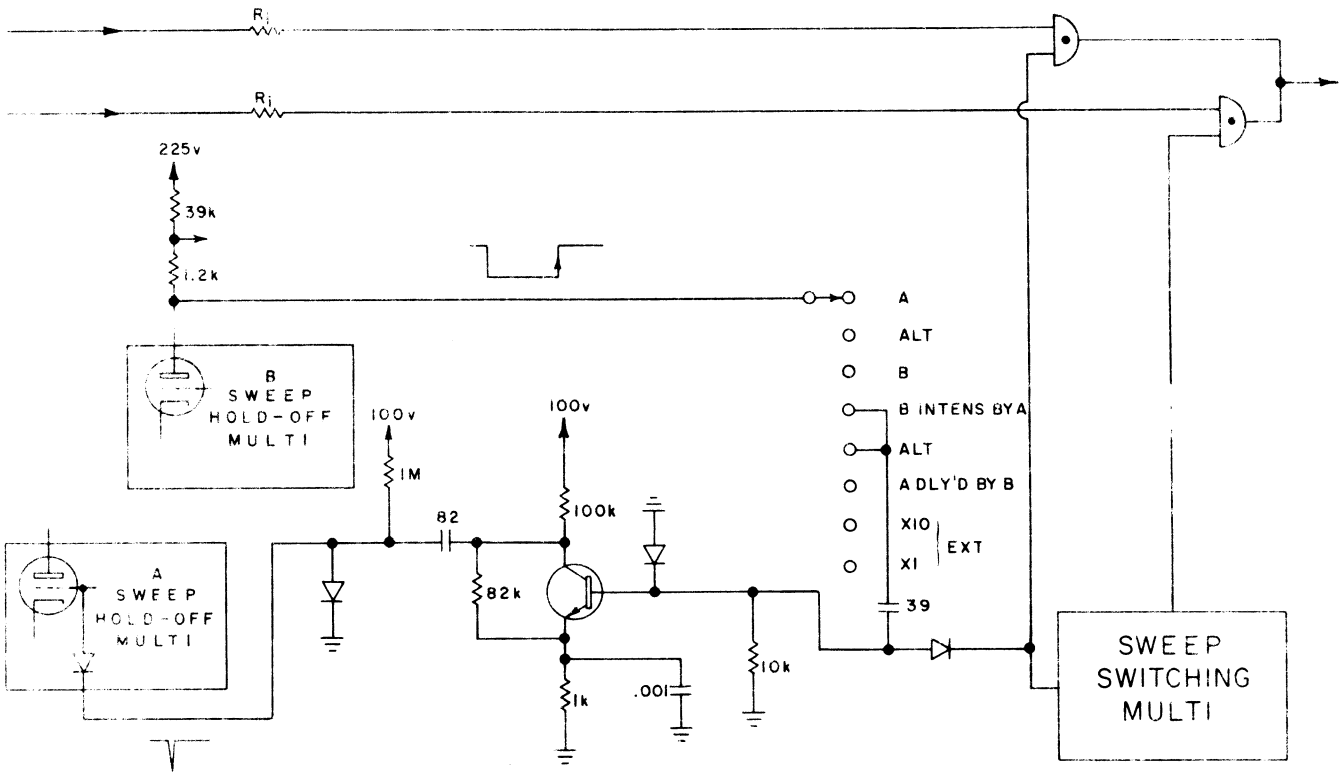
(1) B Sweep ends in the normal manner.

(2) As the B Hold-Off Multi flips and V145A cuts off, a positive step is generated at V145A plate.

(3) The step is differentiated, amplified and inverted in Q444 circuit (Sweep Switching diagram).

(4) The negative pulse pulls down on D347, flipping the A Hold-Off Multi and stopping sweep.

(5) This is called the anti-wrap-around feature.



TYPE 547 SWEEP SWITCHING
ANTI WRAP-AROUND AMPLIFIER

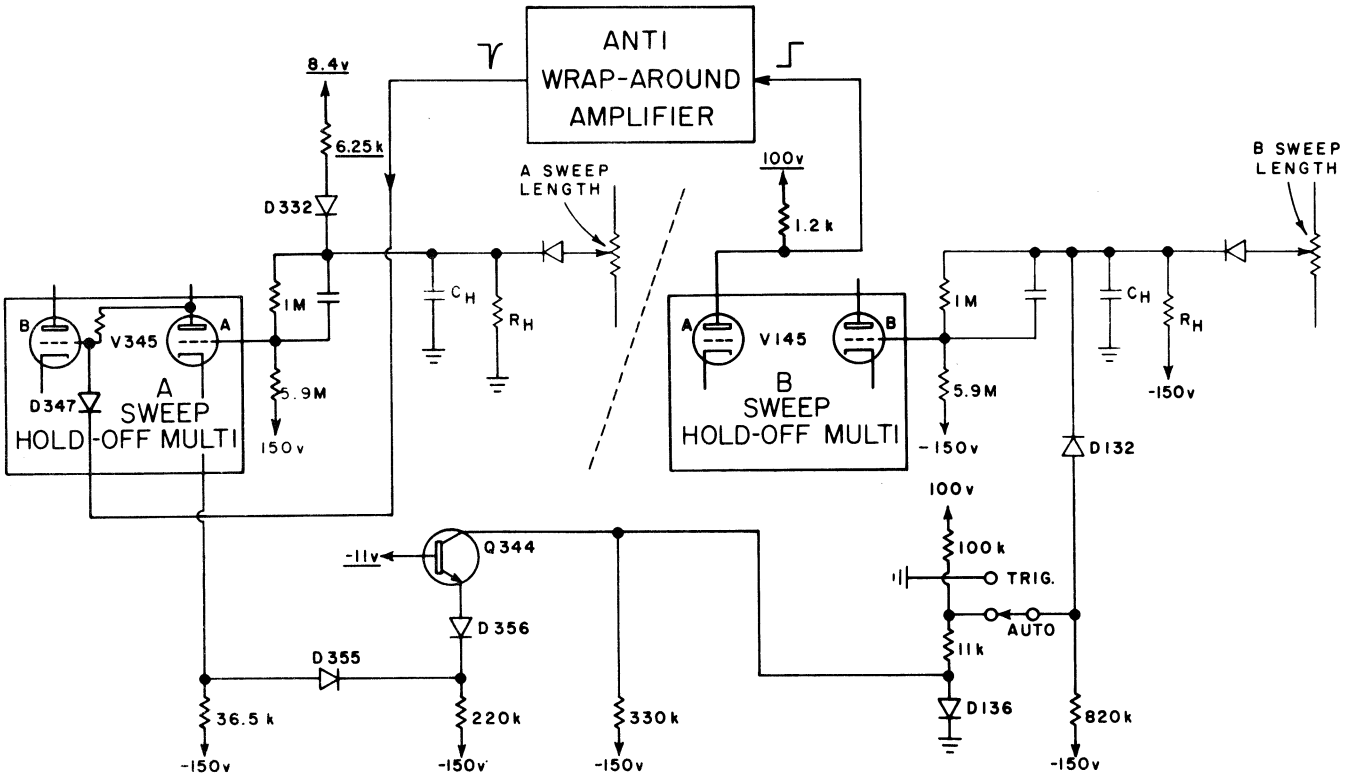
B-547-0030
3-13-'64 dl

g. A and B hold-off begin at about the same time.

(1) Neither sweep can complete hold-off in the normal manner.

(2) A Sweep hold-off bus is clamped at 8.4v.

(3) B Sweep hold-off bus is clamped at 10v.



TYPE 547 HORIZONTAL DISPLAY MODES
B INTEN. BY A, LOCK OUT CIRCUITS (AUTO MODE)

B-547-0079x
4-23-'64 ms

h. As A hold-off reaches its 8.4v level, V345A cathode will have dropped to -12v.

(1) D355 cuts off, D356 turns on, biasing Q344 to saturation.

(2) Q344 collector pulls D132 anode down to 0v.

(3) B Sweep can now complete hold-off.

(4) The B Hold-Off Multi will flip to its ready state.

(5) The next trigger will start another sweep cycle.

8. Circuit conditions in the TRIG mode.

   a. The A Sweep can accept a trigger.

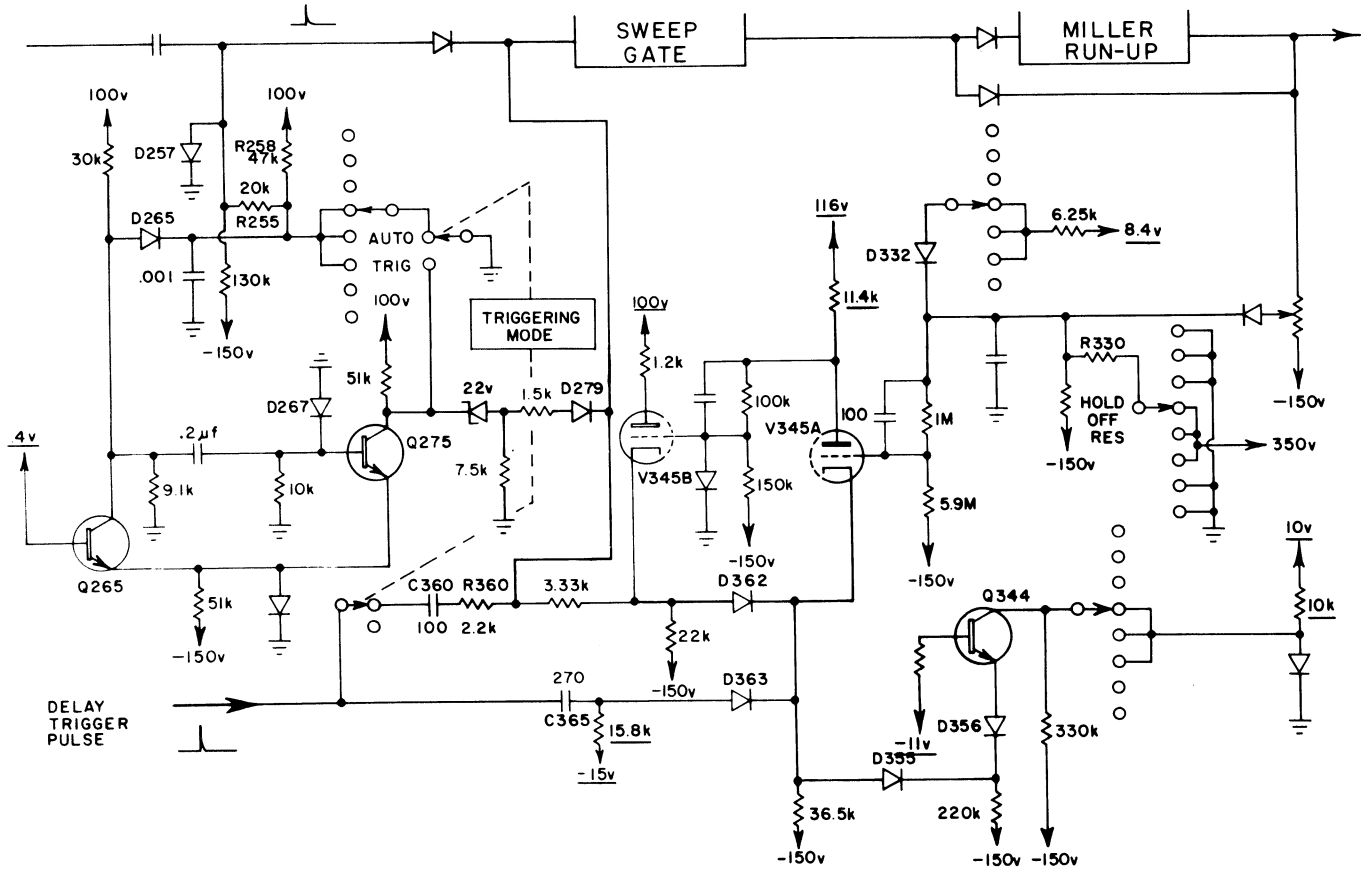
      (1) The ground on R255 is removed.

   b. The Delayed Trigger path through C360, R360 is opened.

   c. D132 anode in the B Sweep hold-off is tied to ground.

   d. A Hold-Off Multi is in its locked out state.

   e. D279 is cut off.



TYPE 547 HORIZONTAL DISPLAY MODES
B INTENSIFIED BY A, A SWEEP

B-547-0077
4-22-'64 jg

9. Operation in the TRIG mode at the start of sweep.

   a. B Sweep is initiated by a trigger.

   b. The Sweep ramp is fed to the Delay Pickoff.

   c. After a calibrated delay, a Delayed Trigger conducted through C365 lifts D363 anode into conduction.

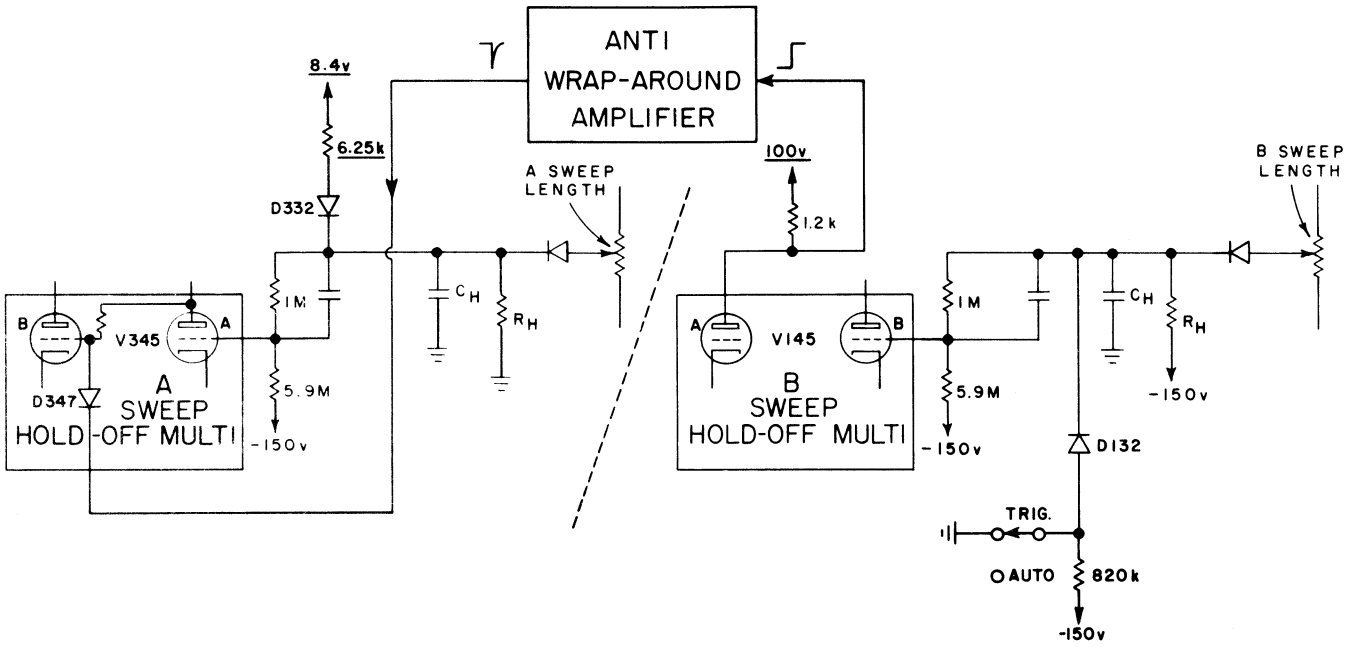
   d. V345A cathode current is directed through D363.

   e. V345A cuts off and the multi flips to its armed state.

   f. The Sweep Gate TD, D285, is in its low state with 4.1 ma flowing.

   g. The next trigger will flip the TD starting sweep.

10. Operation in the TRIG mode at the end sweep.



TYPE 547 HORIZONTAL DISPLAY MODES
B INTEN. BY A, LOCK OUT CIRCUITS (TRIG. MODE)

B-547-0080x
4-24-'64 ms

a. A Sweep ends in the normal manner.

b. A hold-off is clamped at 8.4v so it cannot arm the A Hold-Off Multi.

c. B Sweep and hold-off operate the same as in the normal manner.

   (1) B Sweep does not wait for the end of A hold-off before triggering.

d. If A Sweep does not receive a trigger after being armed (triggers too far apart for the sweep rate), the end of B Sweep disarms the A Hold-Off Multi through D347 and the anti-wrap-around feature.

e. A portion of the A Sweep AUTO-TRIG switch places D132 anode to ground when in the TRIG position.

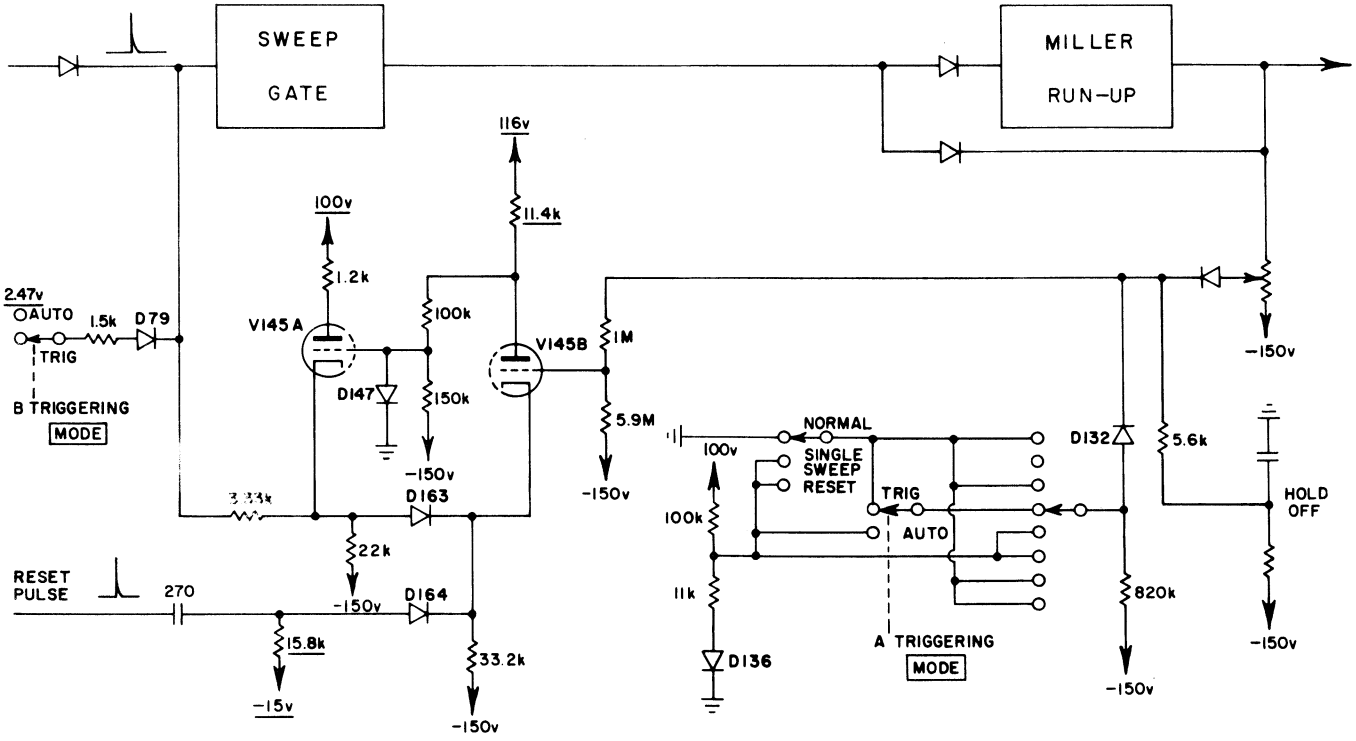
   (1) If D132 anode was connected to Q344 lockout circuit as in the AUTO mode, a condition could develop when no trigger arrives to start A Sweep.

(2) A Sweep Multi is disarmed by a pulse through D347 from the B Hold-Off Multi.

(3) Under this condition, B Sweep lockout would in turn be removed by A Hold-Off Multi turning on Q344.

(4) An accidental interruption during this cycle could lock up the system and the operator would loose trace.

11. Single Sweep Operation



TYPE 547 HORIZONTAL DISPLAY MODES
B INTENSIFIED BY A, SINGLE SWEEP

B-547-0081x
4-23-'64 jg

a. The B Sweep can be armed by the Single Sweep RESET switch while in the B INTENS BY A mode. (A Sweep cannot receive the RESET pulse.)

b. In SINGLE SWEEP mode, the B hold-off bus cannot fall below 10v.

c. The RESET pulse arms the B Sweep circuit (in TRIG mode).

(1) The Ready Light goes on.

d. With the next trigger, B Sweep starts its run up.

e. The Delayed Trigger arrives and A Sweep starts.

f. Both sweeps end like in normal B INTENS BY A operation.

g. In SINGLE SWEEP mode, the connection between Q344 collector and D132 is opened.

(1) The end of A Sweep cannot remove the B Sweep hold-off lockout.

(2) B Sweep can be armed only by a RESET pulse.

C. A DLY'D BY B Mode

1. Operation of A and B Sweeps is essentially the same as in the B INTENS BY A mode.

2. In this mode, however, A Sweep is displayed.

3. The B Sweep Unblanking Gate turns off B Unblanking.

4. The anti-wrap-around feature does not function.

a. The B terminating pulse path from V145A plate is opened.

5. B Sweep can be operated SINGLE SWEEP in the same manner as in B INTENS BY A mode.

D. B INTENS BY A - ALT - A DLY'D BY B Mode

1. This mode alternates B INTENS BY A and A DLY'D BY B modes utilizing switching and logic circuits discussed in the Sweep Switching notes.

E. A - ALT - B

1. Switching and logic circuitry is discussed in the Sweep Switching notes.

F. EXT

1. Both sweep can run either TRIGGERED AUTO or SINGLE SWEEP modes.
2. The sweeps are not displayed, but GATE and SWEEP waveforms are available at the front panel jacks.

TYPE 547

VII. HORIZONTAL AMPLIFIER

A. The Horizontal Amplifier provides a push-pull sweep driving voltage for the horizontal CRT deflection plates.

B. Output is a push-pull voltage ramp 200v peak-to-peak for 10 cm.

1. Nominal CRT deflection sensitivity is 20 v/cm (spec is 18v to 22 v/cm).

2. A sample instrument had a 113v negative going ramp to the left hand deflection plate that ran down from 185v to 72v.

   a. Mid screen potential was 142v.

3. The positive going 110v ramp to the right hand plate ran up from 80v to 190v.

   a. Mid screen potential was 132v.

4. The amplifier is capable of swinging each deflection plate from ground to 330v.

   a. X5 and X10 MAG ranges reach this limit with magnified sweep.

   b. Positioning can also reach these limits with MAG on.

5. Maximum linear sweep rate that can be displayed is 10 nsec/cm.

   a. Range of linearity is over 225 peak-to-peak.

C. Inputs

1. From External Horizontal Amplifier.

2. Sweep ramp from A Sweep Generator.

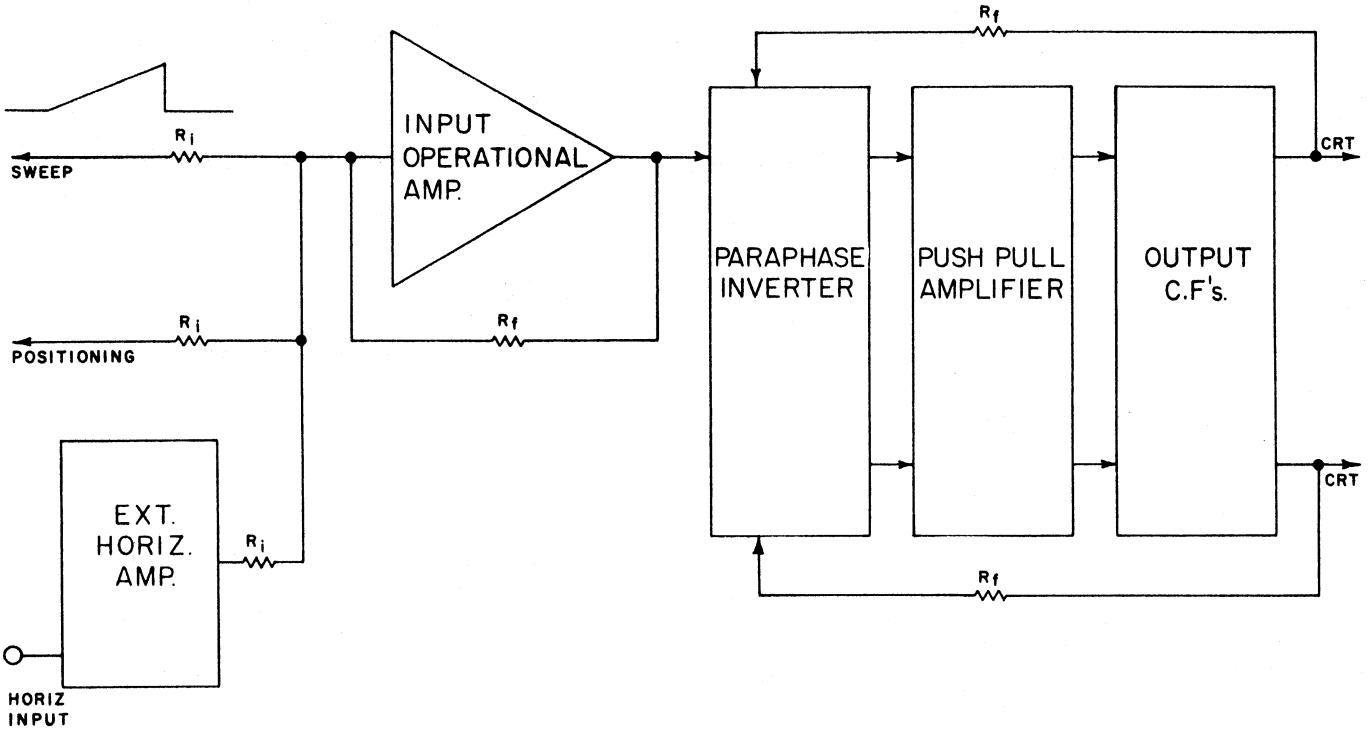
3. Sweep ramp from B Sweep Generator.

4. Positioning information.

D. Magnifier Ranges

1. X1, X2, X5, X10.

E. Block Diagram



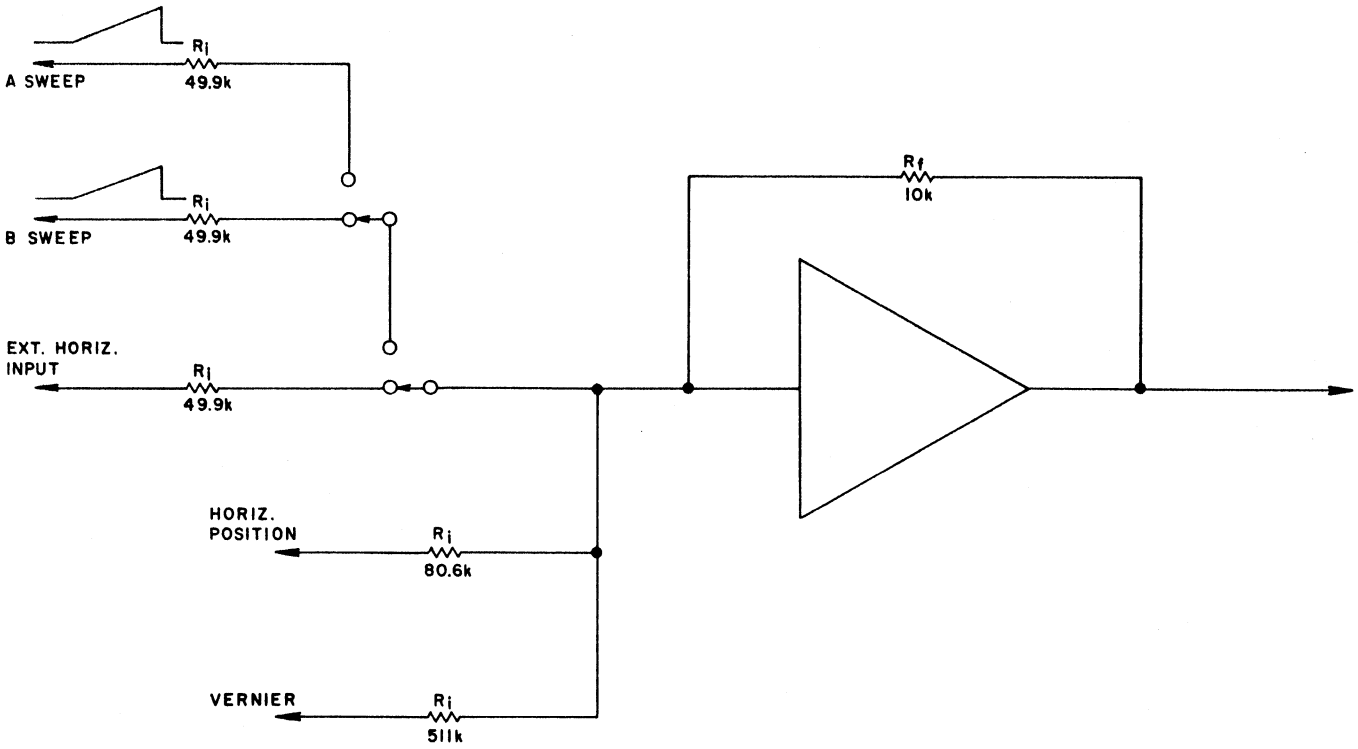
TYPE 547 HORIZONTAL AMPLIFIER
BLOCK DIAGRAM

B-547-0056
4-13-'64 dl

F. Basic Circuits

1. Operational Amplifier
2. Paraphase Inverter
3. Push-Pull Amplifier
4. Output CF's
5. EXT HORIZ Amplifier

G. Basic Operational Amplifier



TYPE 547 HORIZONTAL AMPLIFIER
BASIC OPERATIONAL AMPLIFIER

B-547-0057
4-14-'64 dl

1. The basic operational amplifier is a transistor high gain amplifier.
   a. The operational amplifier provides a low impedance for transmission of the sweep ramp from the sweep deck.
   b. Low signal voltage levels are easier to switch in the Sweep Switching circuit.
2. R_f is composed of R545 and the X10 CAL.

3. There are five Adder inputs (R_i).

   a. 49.9k from the B Sweep Generator (R99).

   b. 49.9k from the A Sweep Generator (R299).

   c. 49.9k from the EXT HORIZ Amplifier (R524).

   d. 80.6k from HORIZ POSITIONING control (R531 and R530A).

   e. 511k from the VERNIER control (R533 and R530B).

4. Operational Amplifier gain = $\frac{R_f}{R_i}$ for $K = \infty$.

   a. For sweep, $A = \frac{10k}{50k}$

   $$A = .2$$

   b. 100v input ramp x .2 = 20v.

   Ramp signal at Q554 base is 20v.

   c. Gain is a function of resistor values and virtually independent of transistor beta.

5. The signal voltage develops across R_f.

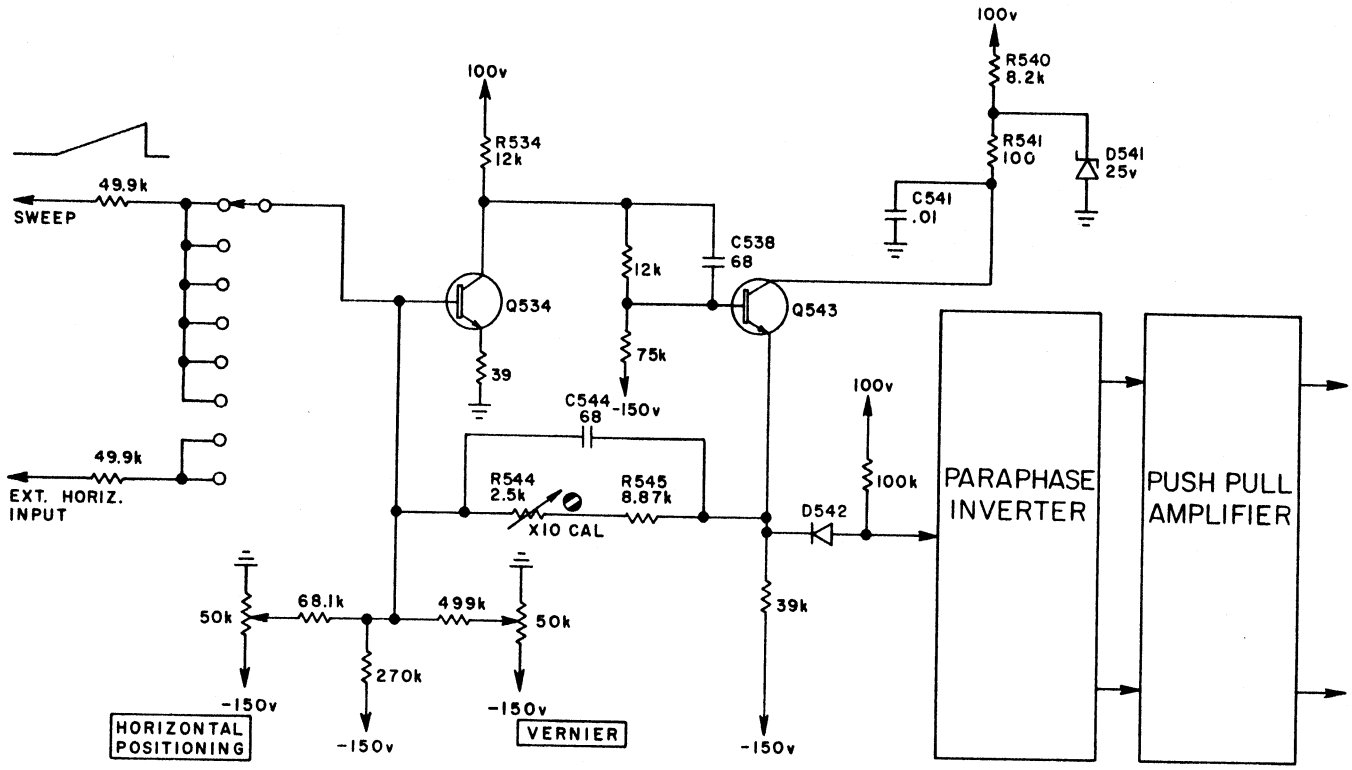
   a. The resultant signal current balances out the input current at the base of the input transistor.

   b. The beedback current at this point is diminished by 1/gain of the stage without feedback.

   c. The result is a very low impedance (virtual ground) at the input transistor base.

6. The input signal current is 200 μa/cm from both sweeps and 20 μa/cm for the EXT HORIZ input.

H. Input Operational Amplifier



TYPE 547 HORIZONTAL AMPLIFIER
INPUT OPERATIONAL AMPLIFIER

B-547-0058x
4-14-'64 dl

1. Two transistors, a Zener and a small signal diode are used in the amplifier.

   a. Q534 is an RCA TA1938 silicon NPN transistor.

   b. Q543 is a Fairchild 2N1893 silicon NPN transistor.

   c. D541 is a Motorola 1M25Z10 10% 25v Zener.

   d. D542 is a Hughes 6075 germanium diode.

2. The two 49.9k R_i resistors for sweep operation are located on the sweep decks.

   a. Sweep inputs to the Horizontal Amplifier are selected by the Sweep Switching circuit.

3. The HORIZONTAL POSITIONING and VERNIER controls are front panel concentric controls.

   a. The HORIZONTAL POSITIONING control has a range of about 11cm.

      (1) Increases with MAG to 110 cm.

   b. The VERNIER control has a range of 1.5 cm.

4. Input from the EXT HORIZ amplifier is selected by the HORIZONTAL DISPLY switch.

5. Q534 base sets close to zero volts with less than a volt of signal.

6. The amplifier signal is taken across Q534 collector load R534.

   a. A divider drops the DC level to near ground.

   b. C538 overcompensates the divider (speed up cap).

7. R545 and the X10 CAL adjust form the R_f for the operational amplifier.

   a. R_f has a value of 10k with R544 at design center.

   b. C544 prevents feedback delay at the start of fast sweeps.

8. Q543, an emitter follower, has a low impedance 25v collector supply.

   a. If Q543 current exceeds 9 ma (or Q543 collector pulls down to ground) D541 disconnects.

   b. R540 limits Q543 collector supply at 25v.

c. Normally D541 clamps the collector supply at 25v.

d. R541, C541 provide decoupling from zener noise.

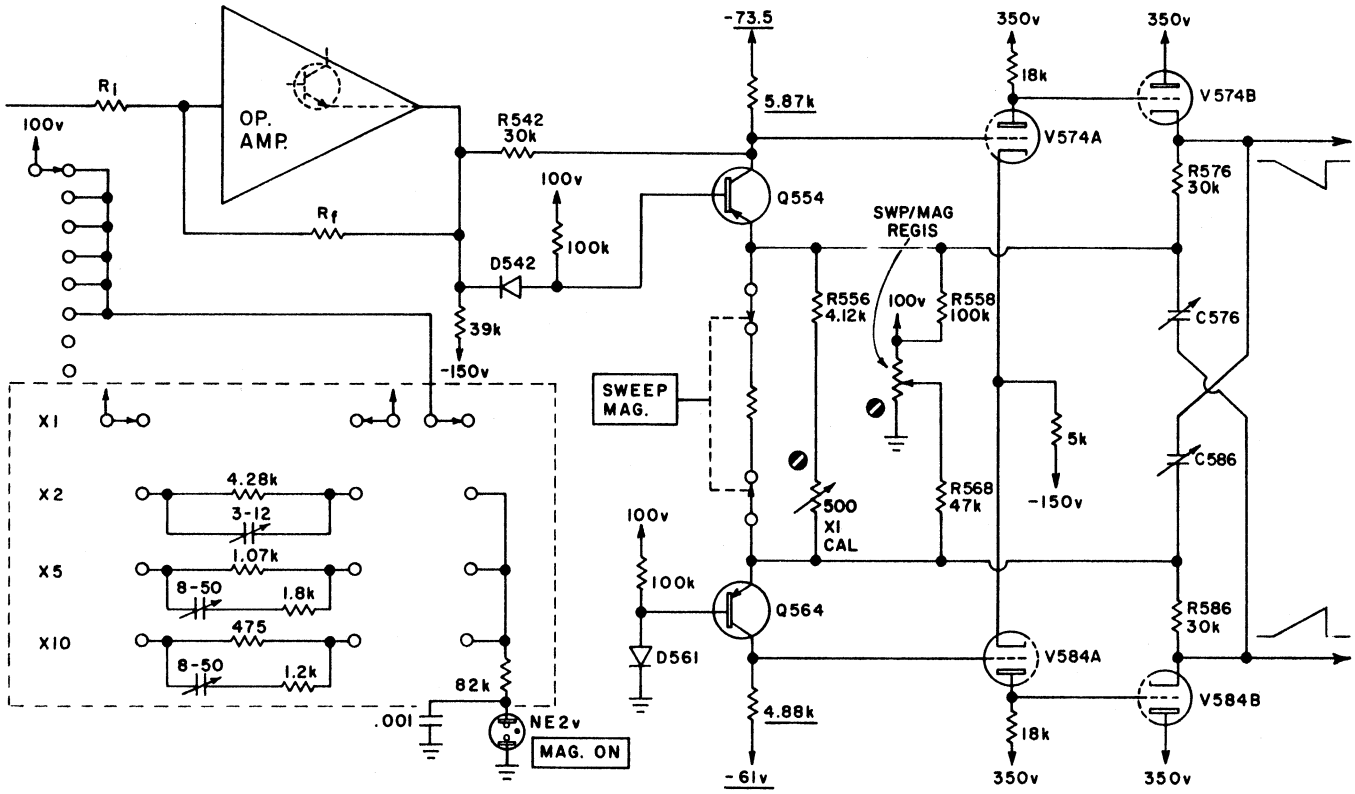
9. Q543 emitter is long tailed to -150v.

10. The operational amplifier output (Q543 emitter) is a negative going sawtooth about 20v peak-to-peak.

a. Center screen voltage is zero.

I. Paraphase Inverter

1. The Paraphase Inverter converts the 20v sawtooth single ended input waveform to push-pull.



TYPE 547 HORIZONTAL AMPLIFIER
PARAPHASE INVERTER

B-547-0059x
4-16-'64 dl

2. The signal from the operational amplifier is a negative going 20v peak-to-peak ramp (2v/cm).
   a. Center screen level on Q554 base is about 0v.
   b. The signal couples through D542 to the base of Q554.
   c. D542 decouples if positioning and sweep raises Q554 base to where base current would exceed 1 ma.
      (1) $B_{V_{EBO}}$ for a 2N2207 is 2v.
      (2) When D542 disconnects, base current is limited by R547 to less than 1 ma.
      (3) This occurs when, with MAG on, the trace is positioned far to the left.
   d. D561 provides temperature compensation for D542.
3. Q554 can saturate at the end of sweep if the trace is positioned far to the right.
4. Q554, Q564 collector resistors are selected to allow negative feedback from Q554 collector to Q543 emitter.
   a. Collector load resistors are equivalent 4.88k to -61v including R542.
   b. Feedback resistor R542 compensates for characteristic unbalance of a paraphase inverter.
   c. The collectors set at about -33v center screen.
   d. The collectors have about a 7v peak-to-peak swing.
      (1) With X10 MAG on, the collector can swing from about -58v to +7v.

(2) Because the feedback loop is broken when the transistors cut off, the collector waveform at the limits of MAG excursion is very ragged.

(3) The displayed portion of the magnified sweep, however, is linear to within 3% for the center 8 cm.

5. At center screen, about 5.7 ma flows through each transistor.

a. 1 ma flows through R558 (and R568).

b. 4.7 ma supplies cathode current through the feedback resistors for the output CF's.

6. Gain of the amplifier is controlled (in the MAG positions) by switching in emitter tying resistors.

a. The tying resistors limit negative feedback (like in the 533/543 Horizontal Amplifier) and limit gain.

(1) The smaller the resistor, the less negative feedback and the greater the gain.

(2) 475 ohm is used in the X10 MAG position.

(3) The X1 position uses only R556 and the X1 CAL resistor that ties the emitters together.

(4) In this position, the X1 CAL controls feedback to adjust gain.

b. An in-phase signal from V574B cathode is fed back through R576 to reinforce the signal on Q554 emitter.

(1) The signal level on the emitter is increased.

(2) Degeneration in the transistor is increased.

(3) Gain of the transistor is decreased.

c. An out-of-phase signal from V384B cathode is fed back through R586 to Q564 emitter.

(1) The driving signal on the emitter is decreased.

(2) The signal on the collector is decreased.

7. The SWEEP/MAG REG adjust balances emitter current in Q554, Q564.

a. The control is most effective when minimum feedback is imposed.

b. It sets the center trace DC level on the CRT plates as MAG is switched on and off.

(1) The center of the trace will not move as MAG is switched off or on.

8. High frequency compensation.

a. Variable high frequency peaking capacitors are provided across the switched-in emitter tying resistors in the MAG positions.

b. A guard voltage is provided by connecting Q543 emitter to wafer 1F-11 of the SWEEP MAG switch.

(1) Capacitance exists from wafer 1R and the switch mounting disc.

(2) Q543 emitter provides a low impedance in-phase drive to wafer 1F physically located between wafer 1R and ground.

c. Positive feedback couples through cross coupled capacitors, C576 and C586, at fast sweep speeds.

(1) The feedback reduces the negative feedback to Q554, Q564 emitters increasing gain.

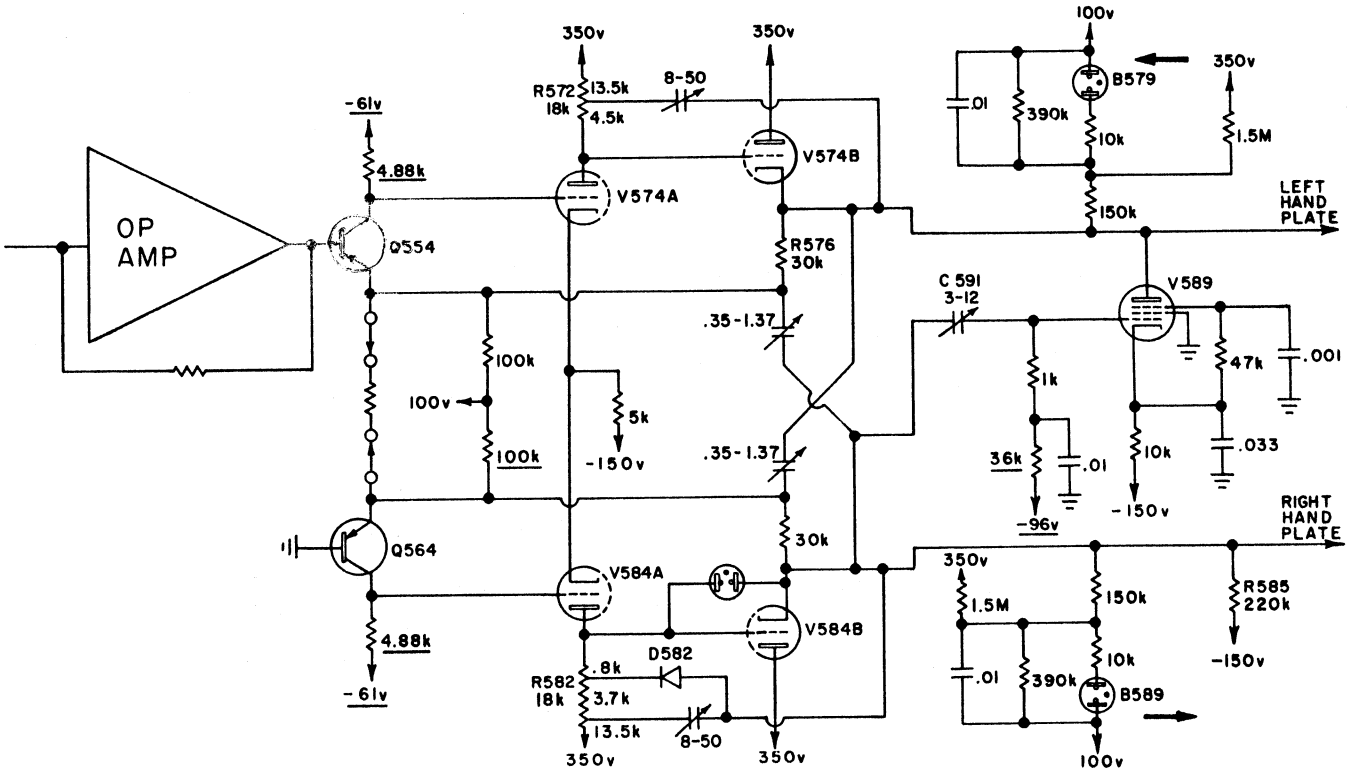
(2) Since the capacitors are variable, they provide an adjustment for high frequency peaking.

9. SWEEP MAGNIFIER switch.

a. The control knob is concentric on the HORIZONTAL DISPLAY switch.

b. A MAG ON light ignites when in any of the three MAG positions.

J. Push-Pull Amplifier and Output CF's



TYPE 547 HORIZONTAL AMPLIFIER
PUSH PULL AMPLIFIER AND OUTPUT C.F's.

B-547-0060x
4-17-'64 dl

1. The push-pull stage contributes most of the Horizontal Amplifier Gain.
   a. It is a cathode coupled push-pull amplifier with a gain of about 15.
   b. Common mode signal is balanced out by the unity coupling.
   c. One amplifier triode V574A and its cathode follower V574B are halves of a 6DJ8.
   d. V584A and V584B are halves of another 6DJ8.
2. At trace center, V574A and V584A grids set at about -33v.
3. With 4v bias, the cathodes are at -29v.
   a. About 12 ma flows through each tube.
4. The plates have about a 110 volt swing from 80v to 190v.
5. Bootstrapping is provided by variable capacitors C572 and C582 to provide high frequency peaking at fast sweep speeds.
   a. Positive feedback, from the cathode follower outputs, couples through the bootstrap capacitors to a tap on the plate load resistors, R572 and R582.
   b. This signal voltage is in phase and about 95% of the amplitude of the signal on V574A (and V584A) plate.
      (1) The figure 95% comes from the average gain of a long-tail CF.
   c. As V374A plate swings positive with large, fast sweeps and the tube approaches cut off, current is supplied through C592.
   d. Bootstrap capacitors are variable to provide HF peaking.

6. The Output CF's provide a low impedance drive to the Horizontal deflection plates.

   a. Deflection plate capacitance is about 2.4 pf per plate.

7. V589 is a high frequency capacitance driver.

   a. V589 is an RCA 6197 pentode.

   b. At fast sweep speeds, the fast negative going sawtooth cuts off V574B.

      (1) The time constant composed of R576 and CRT deflection plate capacitance is not fast enough to follow the fastest sweeps.

      (2) An unexceptably non-linear trace results.

   c. V589 provides the current required to charge the deflection plate capacitance.

      (1) At the faster sweep speeds, where V574B begins to cut off, a positive going sweep ramp is coupled through C591 to drive V589.

      (2) The positive going sweep ramp drives V589 to greater current conduction. The current is provided to charge the deflection plate capacitance.

   d. At fast sweep speeds, the left hand deflection plate is driven through V589.

   e. Since C591 is variable, it can be used to adjust high speed timing.

   f. Linear sweeps of up to 10 nsec/cm can be displayed.

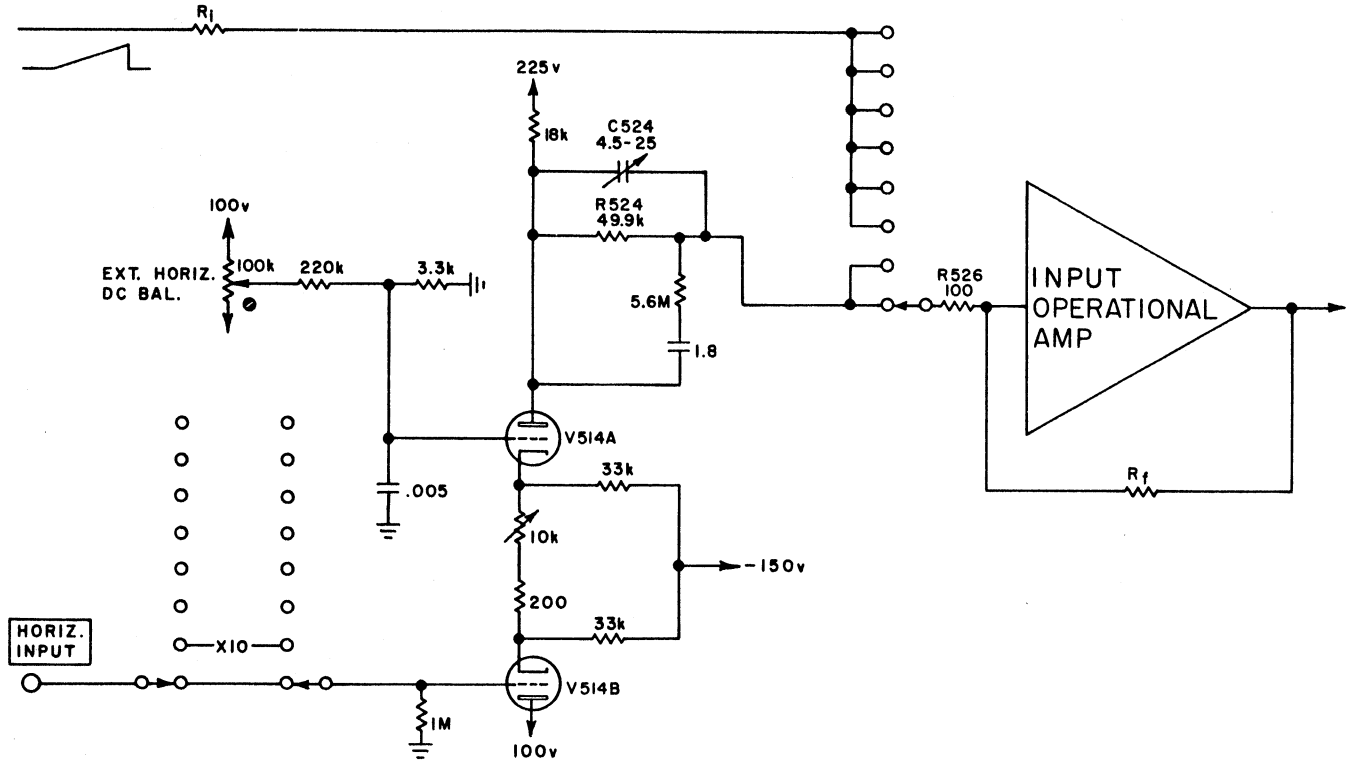
8. D582 and R585 speed up retrace time at fast sweep speeds.
   a. While V574B cuts off during trace time at high sweep speeds, V584B cuts off during retrace.
   b. This does not alter sweep linearity, but at the fastest sweep rates, retrace would exceed hold-off time.
      (1) Hold-off time would have to be extended with a resultant loss of duty cycle.
   c. During retrace, V584B grid drops rapidly and V584B cuts off.
   d. As V584A plate pulls down below V584B cathode, D582 conducts.
      (1) D582 is normally cut off.
   e. Current to charge deflection plate capacitance is supplied by the r_p of V584A and R585.
   f. Linearity is not a factor during retrace - just speed.
9. B583 (a NE-23 neon) protects D582 from reverse breakdown when V584A cuts off.
   a. D582 is a Raytheon 6061 diode with a PIV rating of 200v.
10. In the MAG positions, the output swings from 0v to 330v, limited by the power supply.
11. The position indicator neons show the horizontal position of the beam.
   a. They ignite when the deflection plate potential reaches 185v and extinguish when it drops to 165v.

K. EXT HORIZONTAL Amplifier

1. The External Horizontal Amplifier is a long-tailed cathode coupled amplifier using 6DJ8's.

a. Sensitivity is about 80 mv/cm uncalibrated.

(1) The MAG does not function in EXT HORIZ mode.



TYPE 547 HORIZONTAL AMPLIFIER
EXTERNAL HORIZONTAL AMPLIFIER

B-547-0061x
4-20-'64 dl

2. X1 and X10 (attenuator) inputs are available.
   a. Input impedance is 1 meg at about 50 pf.
      (1) Input Z is not standardized.
   b. The X10 input uses a conventional X10 compensated attenuator.
3. The VARIABLE control has a range of at least 10:1.
   a. Gain is controlled by varying the coupling to the grounded grid stage.
4. The EXT HORIZ DC BAL adjust prevents shift of the CRT beam as the VARIABLE control is rotated.
   a. When properly adjusted, V514A and V514B cathodes set at the same potential.
   b. No static current flows through the VARIABLE control.
   c. With no current through the VARIABLE control, its adjustment cannot effect DC current in V514A or move the beam.
5. The output signal, taken across R522, has a swing of 1v/cm.
   a. The equivalent R_L is 13.2k to 165v.
   b. The voltage drive is converted to a current drive in R524.
   c. The signal current through R526 is 20 μa/cm.
   d. C524 helps standardize input capacitance to the operational amplifier to match that of the sweep inputs.
6. Bandpass limitations.
   a. The bandpass of the external horizontal amplifier is at least 450 kc.
   b. The limitation is imposed by unbypassed cathodes in the cathode coupled amplifier.

(1) Cathodes cannot be bypassed as VARIABLE control would change the time constant with control settings.

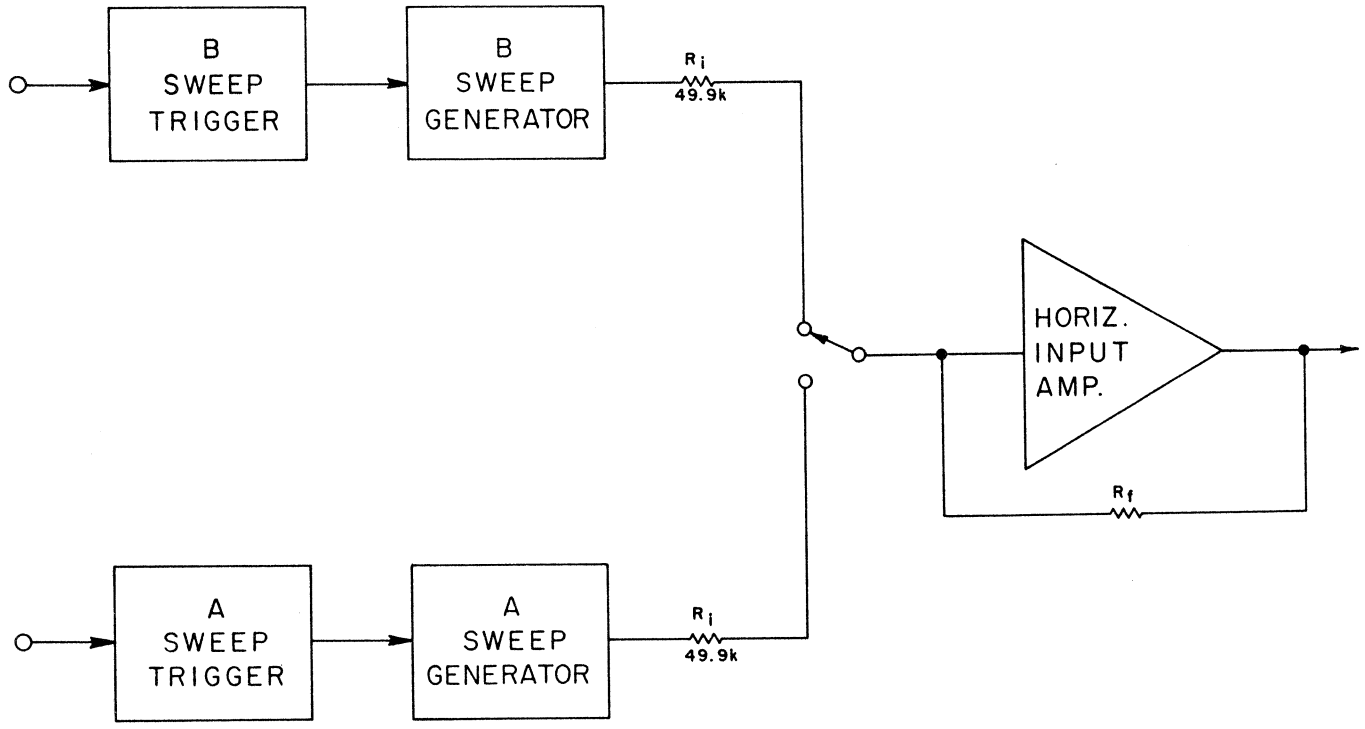
TYPE 547

VIII. ALTERNATE SWEEP SWITCHING

A. The Sweep Switching circuit provides a means by which A and B sweeps can be displayed alternately.

1. The Sweep Switching circuit controls a logic gate which allows a sweep to be displayed.
2. This gate controls the display in all positions of the Horizontal Display switch.

B. Essentially, the Sweep Switching gate can be considered a switch which selects either of the Sweep Generator outputs to feed the Horizontal Amplifier.

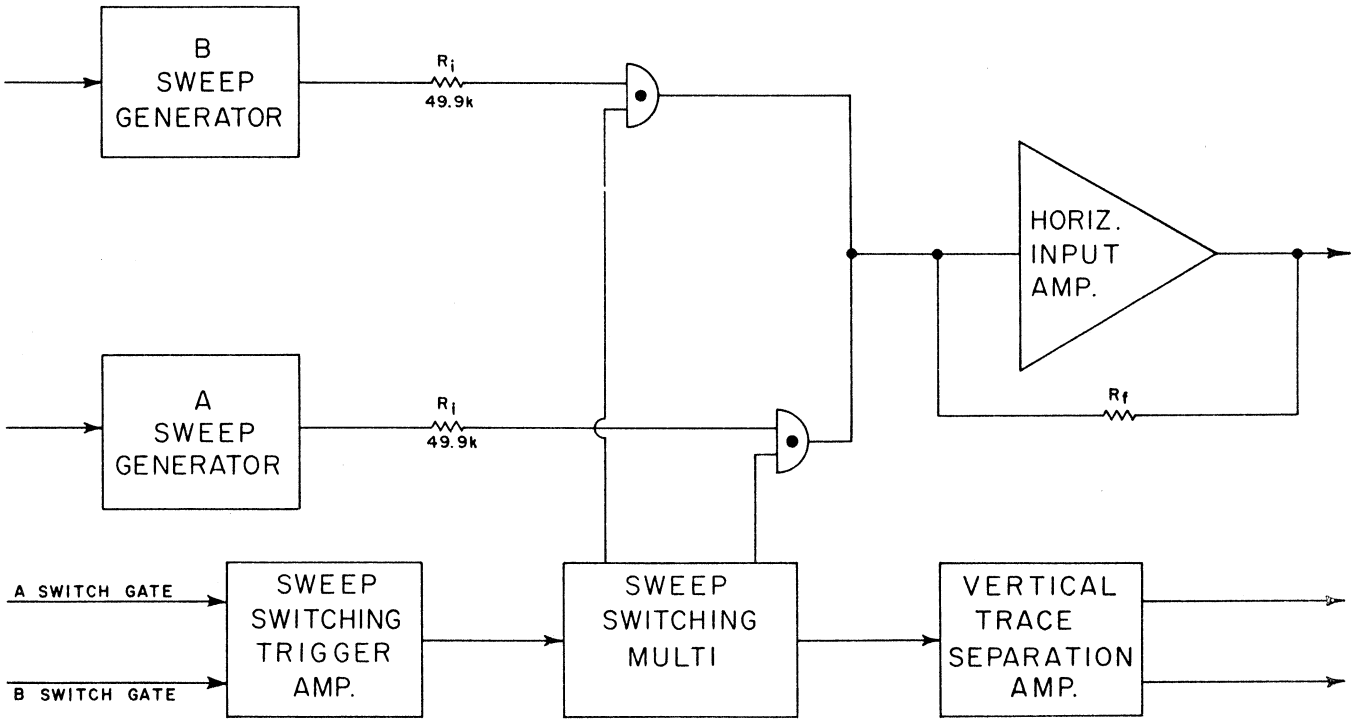


TYPE 547 SWEEP SWITCHING
SYSTEM BLOCK DIAGRAM

B-547-0022
3-5-'64 dl

1. The Horizontal Amplifier Input is an Operational Amplifier.
2. The R_i's for the Operational Amplifier are shown as part of the Sweep Generator Circuits.
   a. R_i's are 49.9k resistors.
   b. The input voltage waveform is the 100v sweep sawtooth (10v/cm) output from the A and B Sweep Generator.
   c. The voltage waveform is converted in R_i to a current sawtooth of 200 μa/cm.
   d. It is the current waveform that is switched in the Logic Gate -- the voltage waveform is about 150 mv.

C. Block Diagram



TYPE 547 SWEEP SWITCHING BLOCK DIAGRAM

B-547-0023
3-5-'64 dl

D. Block Logic

1. The two outputs from the Sweep Switching Multi are either at ground or +27v.

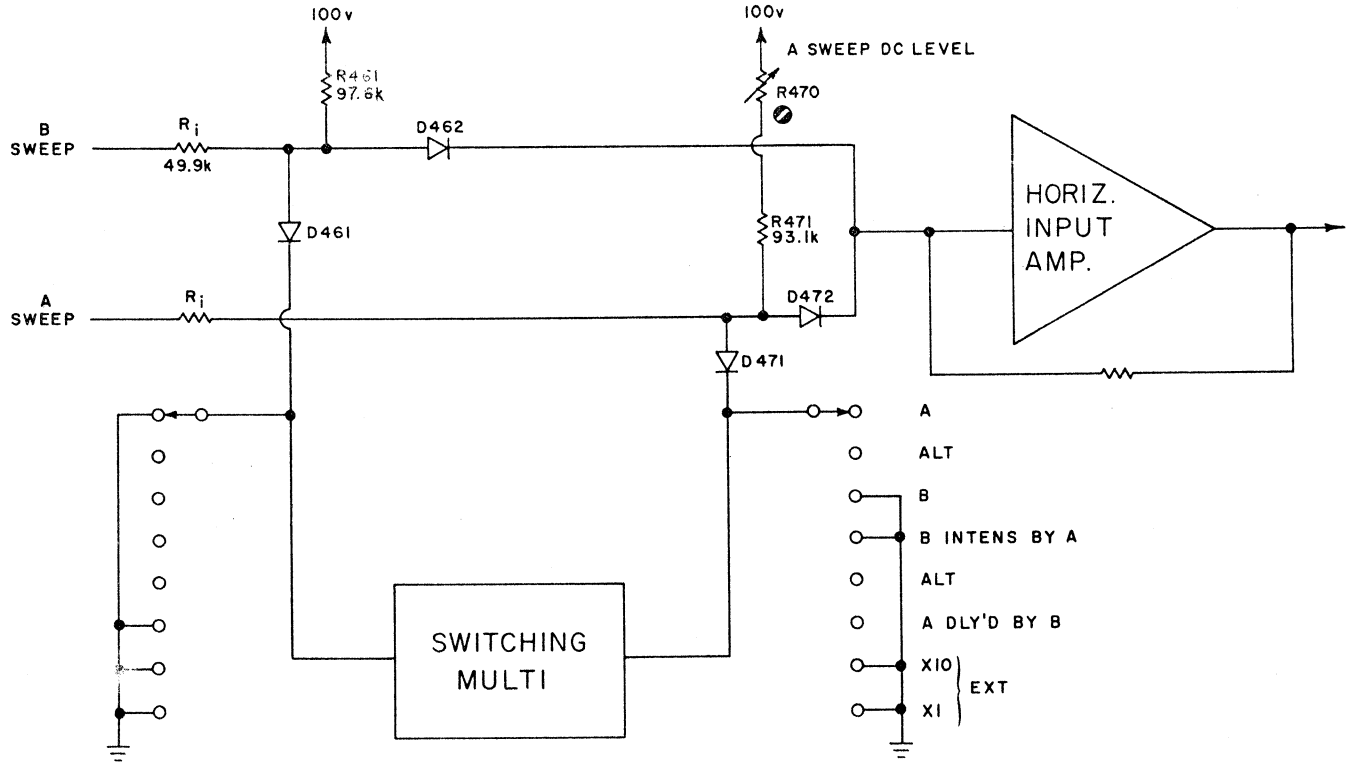
   a. Only one output can be at 27v at a time.

2. When an output is at 27v, the logic gate will pass the sweep signal to the Horizontal Amplifier.

3. A positive going step at the end of sweep is amplified and inverted in the Sweep Switching trigger amplifier and fed to the Switching Multi.

4. As the Switching Multi gates on the A sweep, the Trace Separation circuit displaces the A sweep display on the screen by a controlled amount.

E. Switching Gates



TYPE 547 SWEEP SWITCHING
SWITCHING GATES

B-547-0024x
3-6-'64 dl

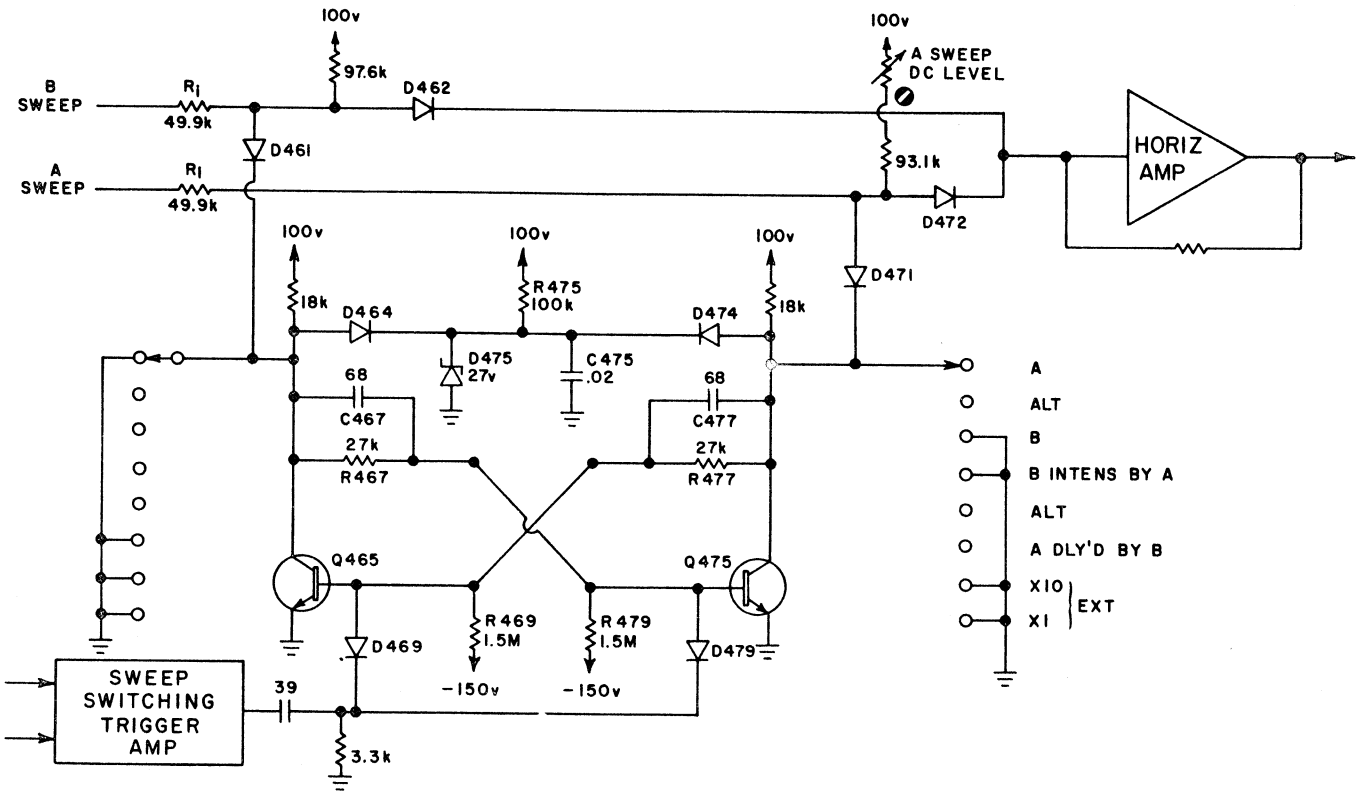
1. The switching gates are composed of TEK made GaAs diodes (D462 and D472) and GE 1N3605 silicon diodes (D461 and D471).
2. Consider the condition when the HORIZONTAL DISPLAY switch is in the A position (or A DLY'D BY B).
   a. The left side of the Switching Multi is grounded through the HORIZ DISPLAY switch.
      (1) The Multi is forced to remain in one state.
   b. The right side of the Multi then is at 27v.
   c. With D461 cathode at ground, the diode conducts, pulling D462 anode down to .6v.
   d. D462 cuts off.
   e. The B sweep signal current passes through D461 to ground.
   f. With D471 cathode at 27v, the diode is cut off.
   g. D472 is held in conduction by current through R470 and R471.
   h. A sweep signal current passes through D472 to the Horizontal Amplifier.
3. When the HORIZONTAL DISPLAY switch is in the B position (or B INTENS BY A), the right side of the Multi is grounded, cutting off D472.
   a. The left side of the Multi is at 27v, allowing D462 to conduct and pass the B sweep signal to the Horizontal Amplifier.
4. In the two ALT positions, the Multi flips at the end of the last sweep.
   a. Alternate sweeps are displayed.

5. In the EXT positions, both sides of the Multi are grounded.

   a. Both D462 and D472 are cut off and horizontal display switch disconnects Switching Gate.

   b. Neither sweep can pass to the Horizontal Amplifier.

F. Sweep Switching Multi



TYPE 547 SWEEP SWITCHING
SWITCHING MULTI

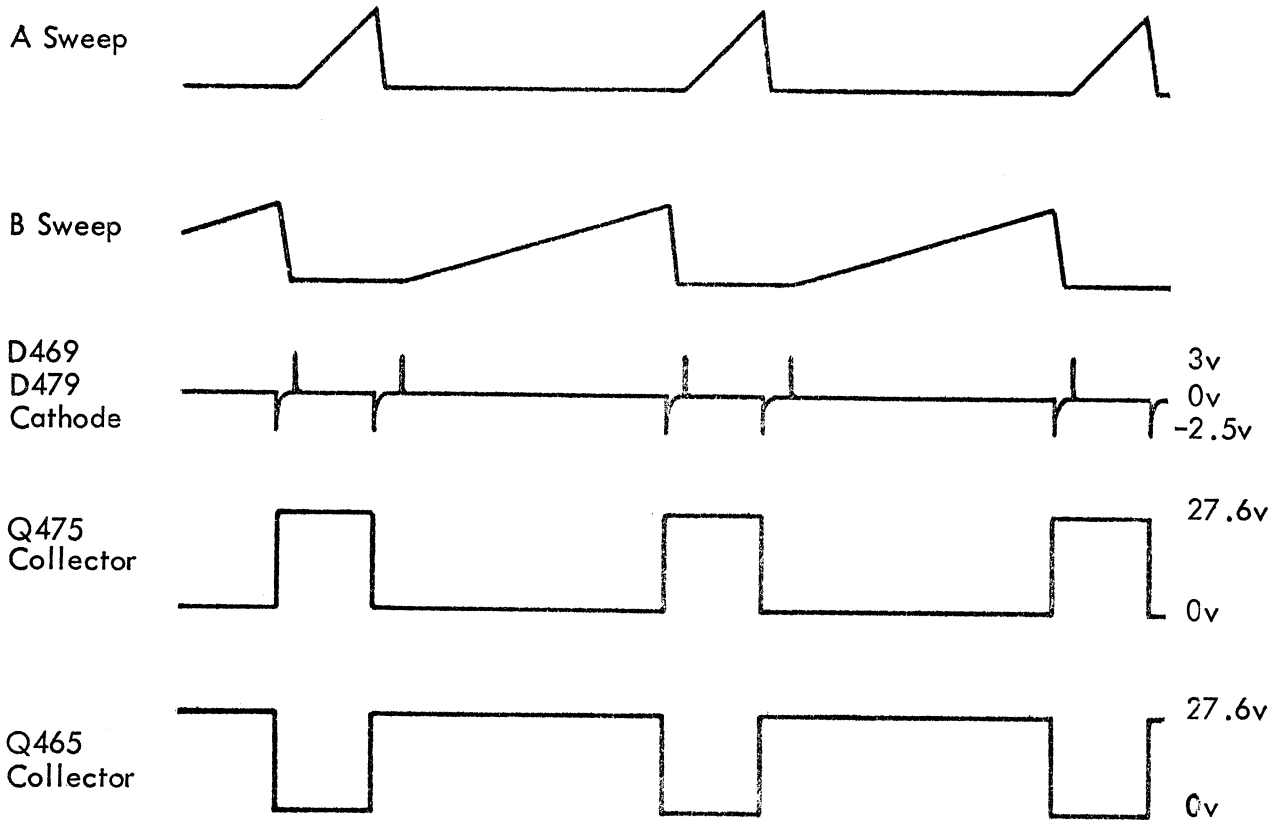
B-547-0025x
3-9-'64 dl

1. The Sweep Switching Multi is a transistorized bistable Eccles Jordan multi.*
2. The transistors are 151-108 selected Motorola 2N2501 silicon transistors.
3. Four diodes and a zener are used.
   a. The diodes are GE 1N3605 silicon diodes.
   b. D475 is a Motorola 1N971B 5% 27v zener.
4. The conducting transistor has its collector pulled down to ground.
5. The cut-off transistor has its collector caught by D464 or D474 at 27.6v.
   a. D475 clamps the D464 and D474 cathodes at 27v.
   b. R475 provides current for D475.
   c. C475 bypasses zener noise.
6. A bistable multi, by definition, requires a trigger to flip it to each of its stable states.

* Typical Oscilloscope Circuitry, Page 10-18.

7. Sequence of operation.

a. The steering diodes, D469 and D479, conduct the trigger to whichever transistor is conducting.



SCOPE UNDER TEST	FREE RUN
MODE: A ALT. B	
A SWEEP: 10 μ sec/cm	
B SWEEP: 20 μ sec/cm	
TEST SCOPE: .1 msec/cm	

b. The cut-off transistor has its collector at 27.6v.

(1) The divider composed of R467 (or R477) and R469 (or R479) supplies adequate base current to the conducting transistor.

c. The conducting transistor has its collector at ground.

(1) The divider sets the base of the cut-off transistor at -2.4v.

(2) -2.4v on the base assures cut-off of the transistor and its steering diode.

d. Base current then for the conducting transistor flows through R467 (or R477).

e. The negative going trigger conducted through a steering diode pulls down on the base of the conducting transistor.

f. As the transistor cuts off, the Multi flips.

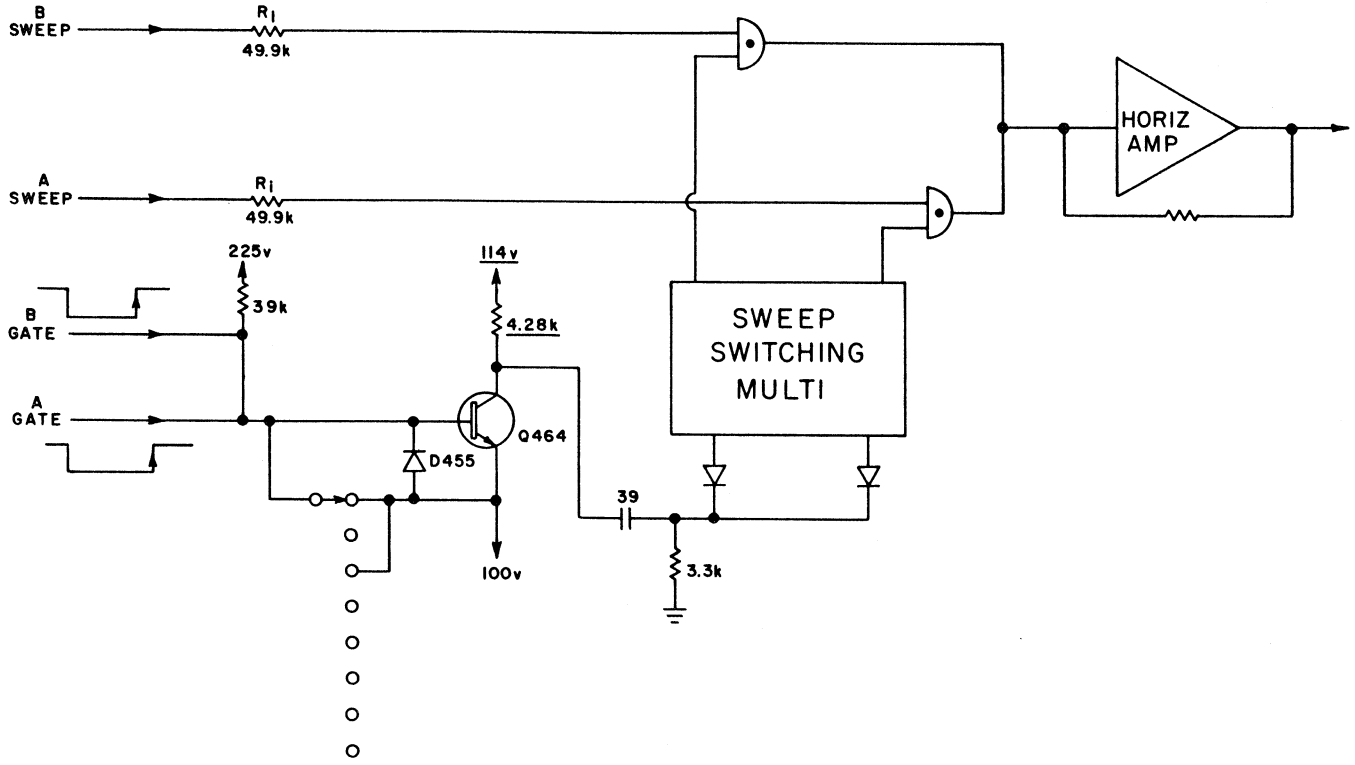
g. The Multi will remain at this state until the arrival of the next trigger which again switches the Multi.

8. C467 and C477 are speed-up capacitors to assure fast Multi switching.

a. Also provide memory to the Multi as to which side was conducting.

G. Switching Trigger Amplifier

1. The Multi Trigger Amplifier provides a negative-going trigger to switch the Sweep Switching Multi.



TYPE 547 SWEEP SWITCHING
SWITCHING TRIGGER AMPLIFIER NO.1

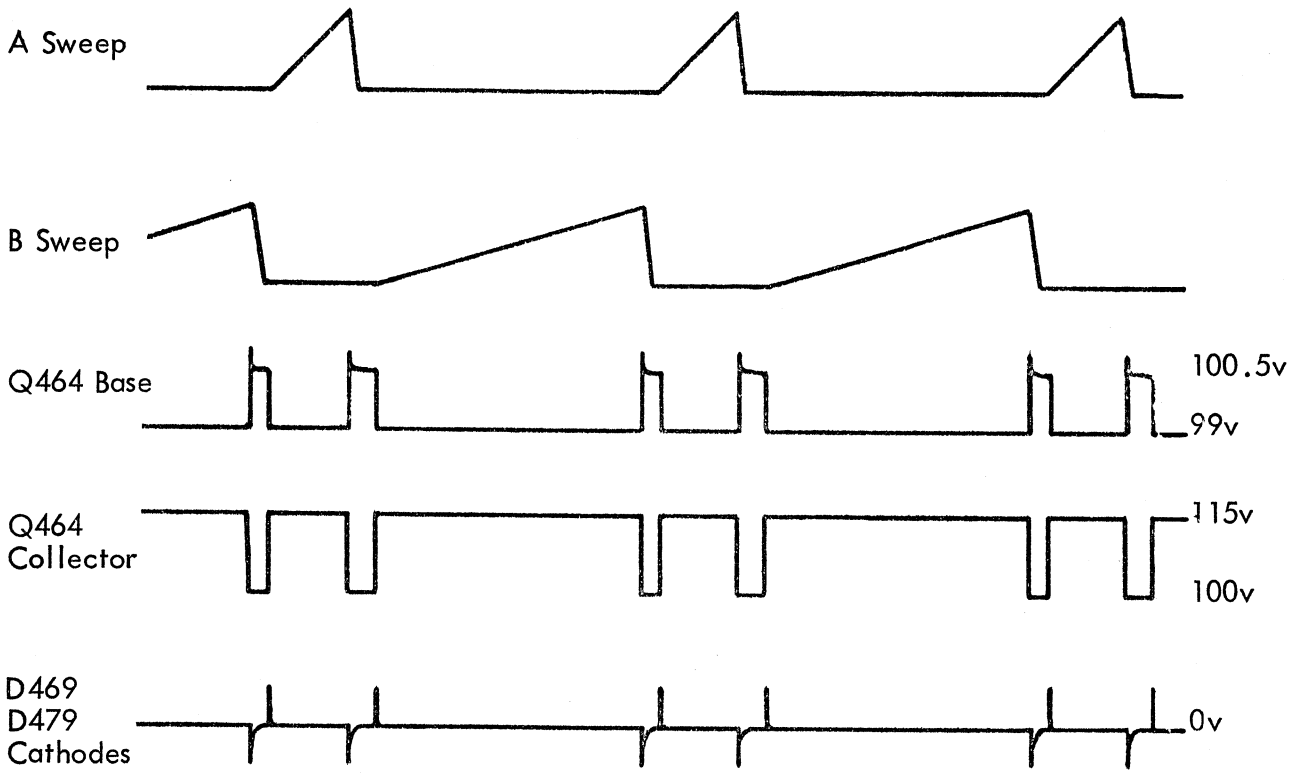
B-547-0026x
3-9-'64 dl

2. The circuit uses a 151-108 NPN silicon transistor and a GE 1N3605 silicon diode.

3. In the A and B positions of the HORIZONTAL DISPLAY switch, the base and emitter are shorted -- the transistor is cut off.

   a. In all other switch positions, the amplifier functions.

4. In the quiescent condition (during sweep), Q464 is cut off.



SCOPE UNDER TEST	FREE RUN
MODE: A ALT. B	
A SWEEP: 10 μ sec/cm	
B SWEEP: 20 μ sec/cm	
TEST SCOPE: .1 μsec/cm	

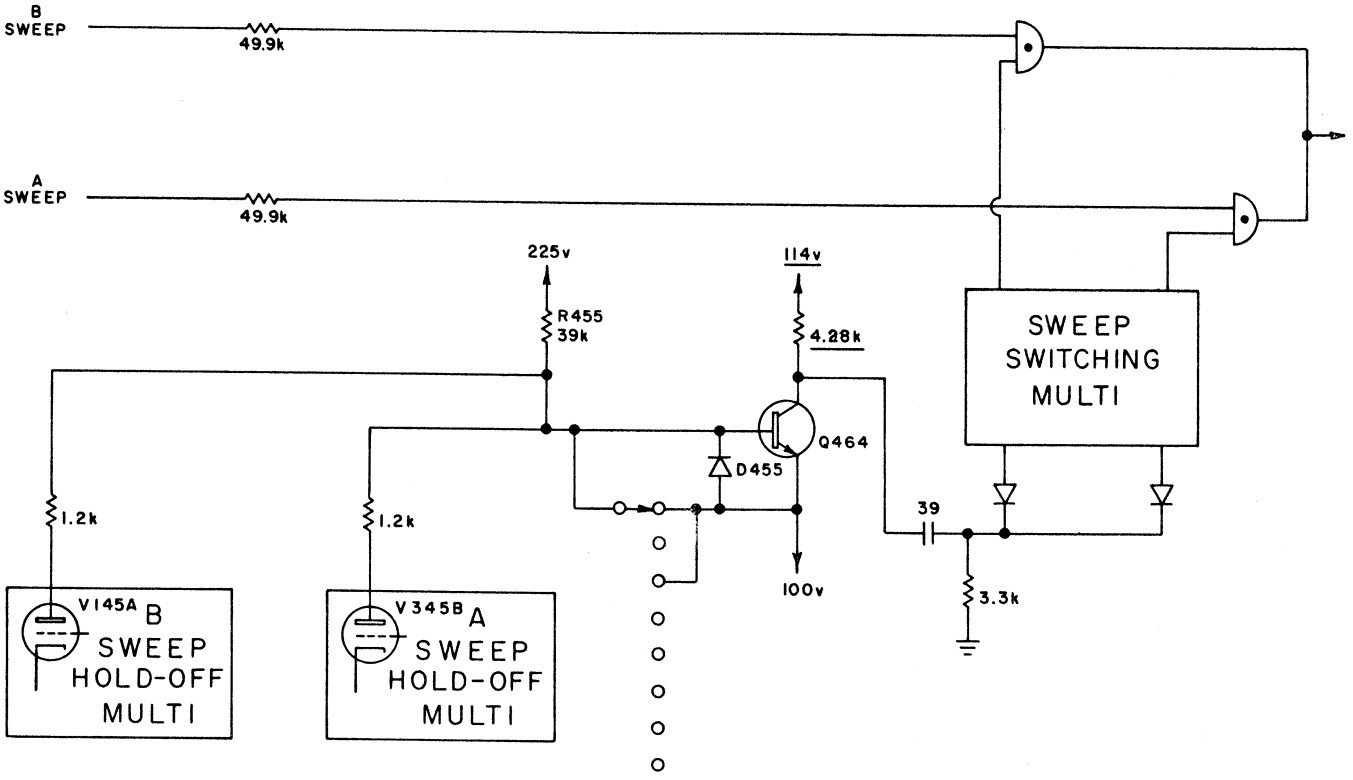
5. The 1.5v positive going pulse on the base biases the transistor to saturation.

   a. The collector drops from 114v to 99v for the pulse duration.

   b. The equivalent collector load is 4.28k to 114v (R458, R457 equivalent).

6. D455 keeps Q464 base from dropping below 100v during the time both A and B sweeps are running simultaneously.

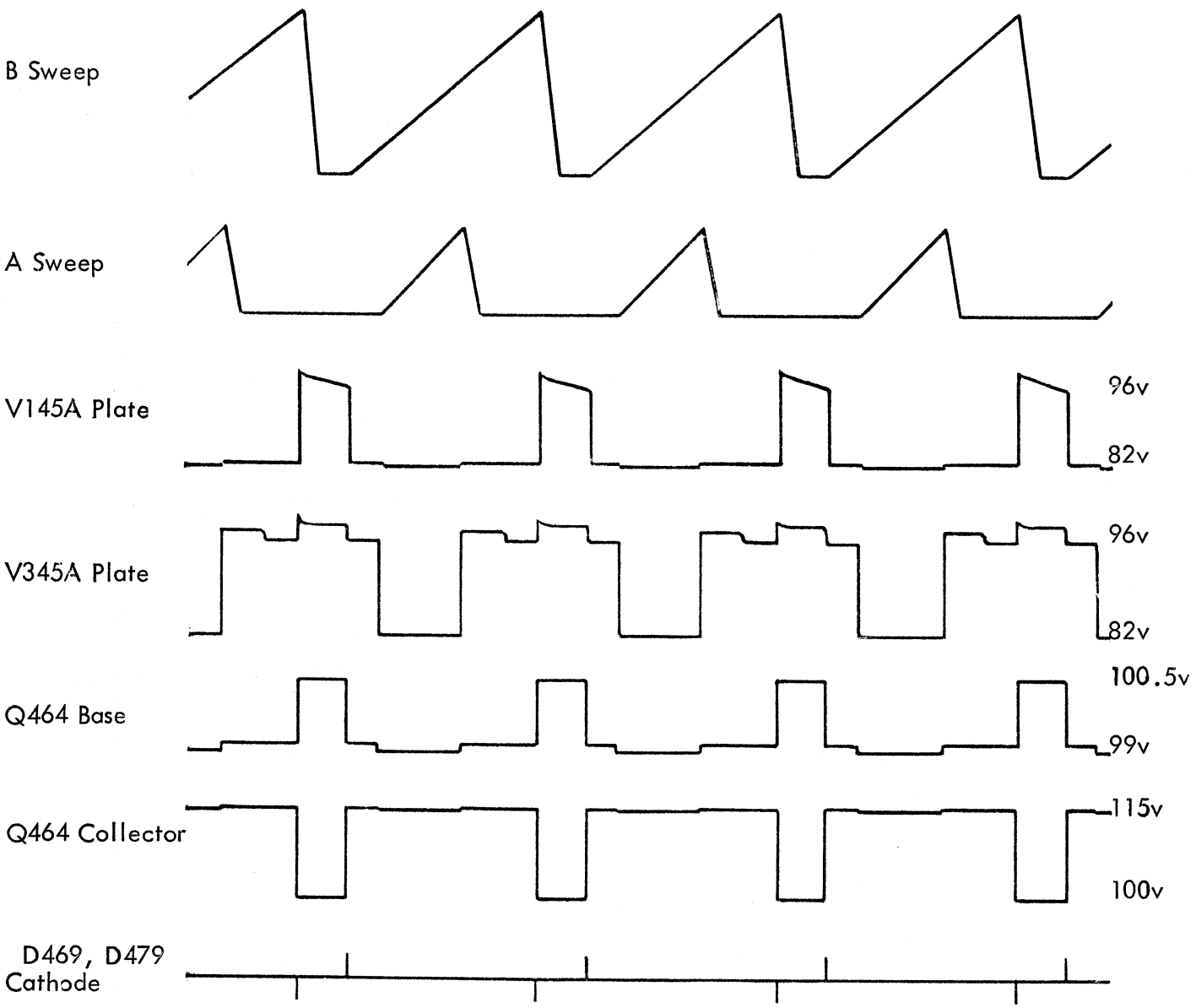
H. Source of Sweep Switching Trigger



TYPE 547 SWEEP SWITCHING
SWITCHING TRIGGER AMPLIFIER NO. 2

B-547-0027x
3-10-'64 dl

1. R455 provides a common current source for both V154A and V345B.
   a. V154A is the left triode in the B Sweep Hold-Off Multi.
   b. V354B is the left triode in the A Sweep Hold-Off Multi.
   c. These tubes conduct except during hold-off time for their respective sweeps.



SCOPE UNDER TEST	FREE RUN
MODE: DLY'D. ALT.	D.T.M. 140
A SWEEP: 10 μ sec/cm	
B SWEEP: 20 μ sec/cm	
TEST SCOPE: .1 msec/cm	

2. Since (in DLY'D ALT) both sweeps would be running (with some arbitrary time sequence) when Sweep Switching is required, the waveform on Q464 base would be the algebraic sum of the two plate waveforms.

a. During the time that both tubes are conducting, however, D455 limits the negative waveform excursion to 100v.

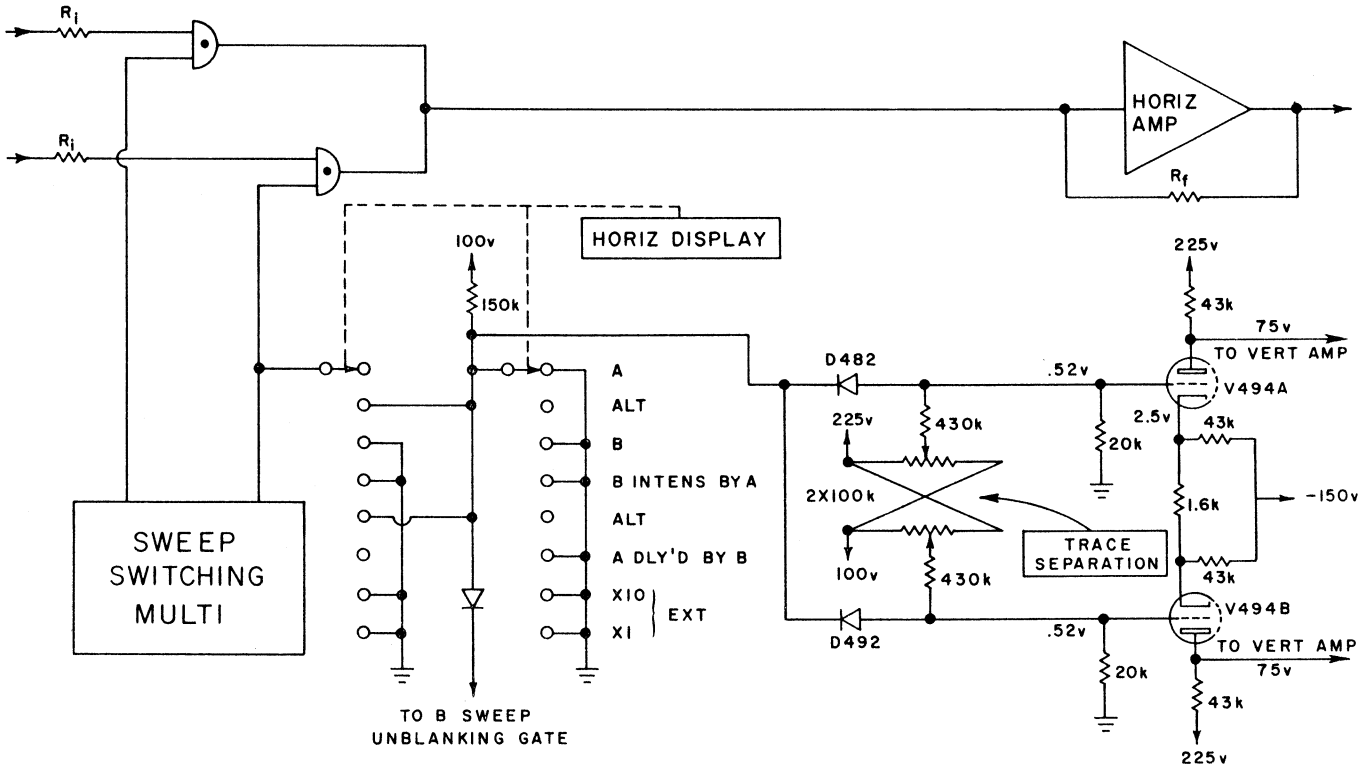
b. When either V154A or V354B or both are conducting, Q464 base sets at 100v.

c. When both are cut off, the current from R455 is diverted to the base of Q464.

d. The resultant current switch is the trigger that switches the Sweep Switching Multi.

I. Trace Separation Amplifier

1. The Trace Separation circuit provides a method of positioning the A trace relative to the B trace while in the ALT modes.



TYPE 547 SWEEP SWITCHING
TRACE SEPARATION AMPLIFIER

B-547-0028x
3-11-'64 dl

2. The circuit is a push-pull DC amplifier using two halves of a 6DJ8.
   a. The output drives into a grounded base circuit in the Vertical Amplifier.
   b. Any difference in current through the amplifier plate load will result in a vertical shift in trace position.
   c. The plates are connected (in the Vertical Amplifier circuit) through 5.1k resistors to the emitter of the grounded base amplifier.
   d. Under normal conditions, there is no voltage drop across the 5.1k resistors so no current is supplied.
   e. The plates, therefore, see only the 43k plate load resistors.
3. In all except the two ALT modes, the circuit input (D482 and D492 cathodes) is grounded through the HORIZONTAL DISPLAY switch.
4. In the two ALT modes, the input is tied to the right hand output (the output that drives the A Sweep Switching Gate) from the Switching Multi.
   a. When A sweep is being displayed, the Multi output is at 27v.
5. In the quiescent condition (D482 and D492 cathodes at ground; either grounded by the DISPLAY switch or by action of the Switching Multi), both diodes are conducting.
   a. Each diode is held in conduction by about 350 μa through an equivalent 20k to 7v.
   b. With both grids clamped to 0v, the plates are at the same level and no trace shift occurs.

6. When A sweep is displayed in the ALT modes, D482 and D492 cathodes are raised to 27v.
   a. The diodes cut off.
   b. The grids are now free to seek the levels set by the TRACE SEPARATION control.
   c. The control can swing each grid from 4.5v to 10v.
   d. Actually, the grid swings from .6v during B sweep display to a voltage (4.5v to 10v) selected by the TRACE SEPARATION control during the time A sweep is displayed.
7. The amplifier is a cathode coupled long-tail push-pull amplifier so signal coupling occurs between cathodes.
   a. With long-tail cathode returns, it can be considered a constant current circuit.
   b. There is virtually no difference in plate current with both grids at 6.5v (design center on the TRACE SEPARATION control) and a .6v.
   c. Considering the input waveform as a square wave, the 6.5v (control design center) signal appears on the grids as a common mode signal.
      (1) The grids move together.
      (2) There is no output at the plates.
   d. As the control is rotated, the tube with the more positive grid will control the output.
      (1) The tube with the less positive grid will appear to have no polarity reversal; the plate will swing in the same direction as the grid.
      (2) Actually, the signal drive is through its cathode.

e. As the control is rotated, the plates will move above 75v by about 10v and below 75v by about 12v.

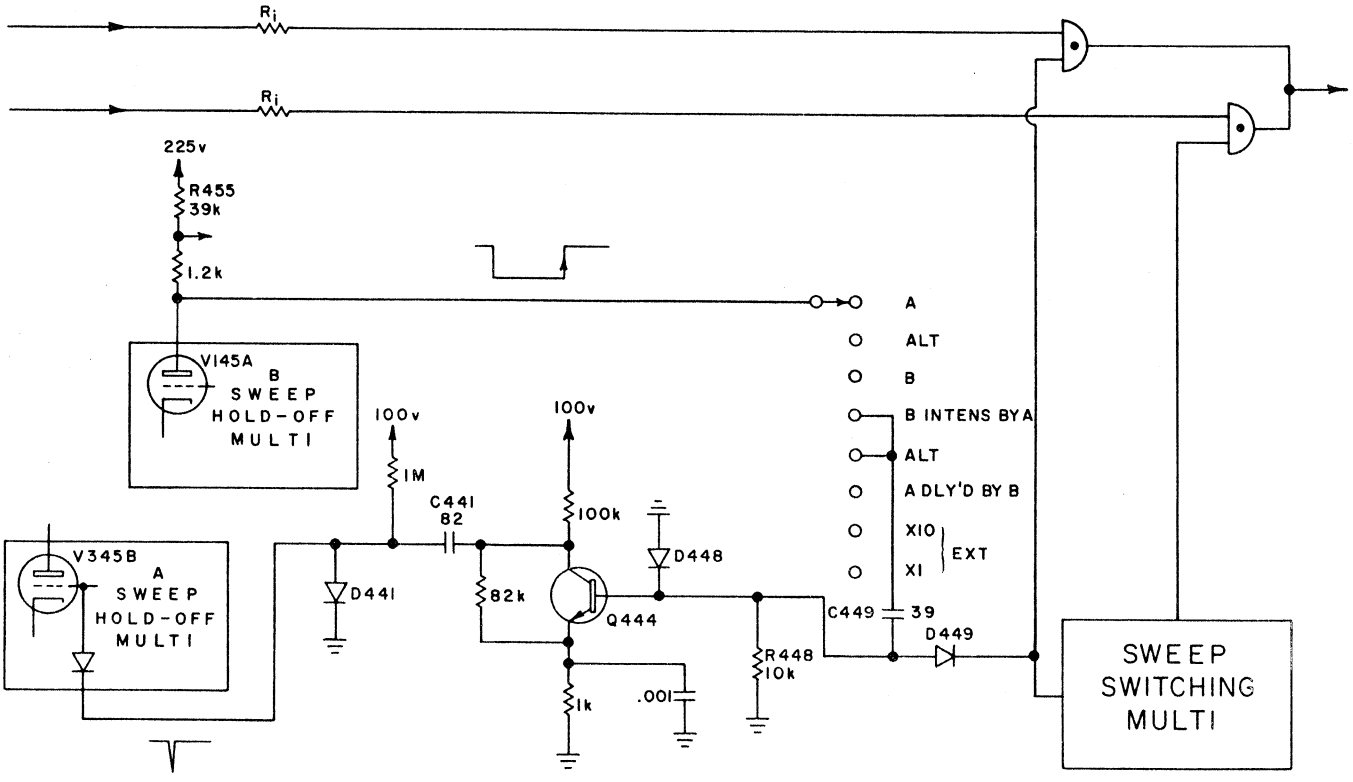
(1) A maximum of ±4 ma can flow to each side of the Vertical Amplifier.

J. Anti-Wrap-Around Amplifier

1. The circuit prevents the A intensified zone from extending beyond the end of B sweep.

a. It functions only in the B INTENS BY A mode or when B INTENS BY A is displayed in the ALT mode.

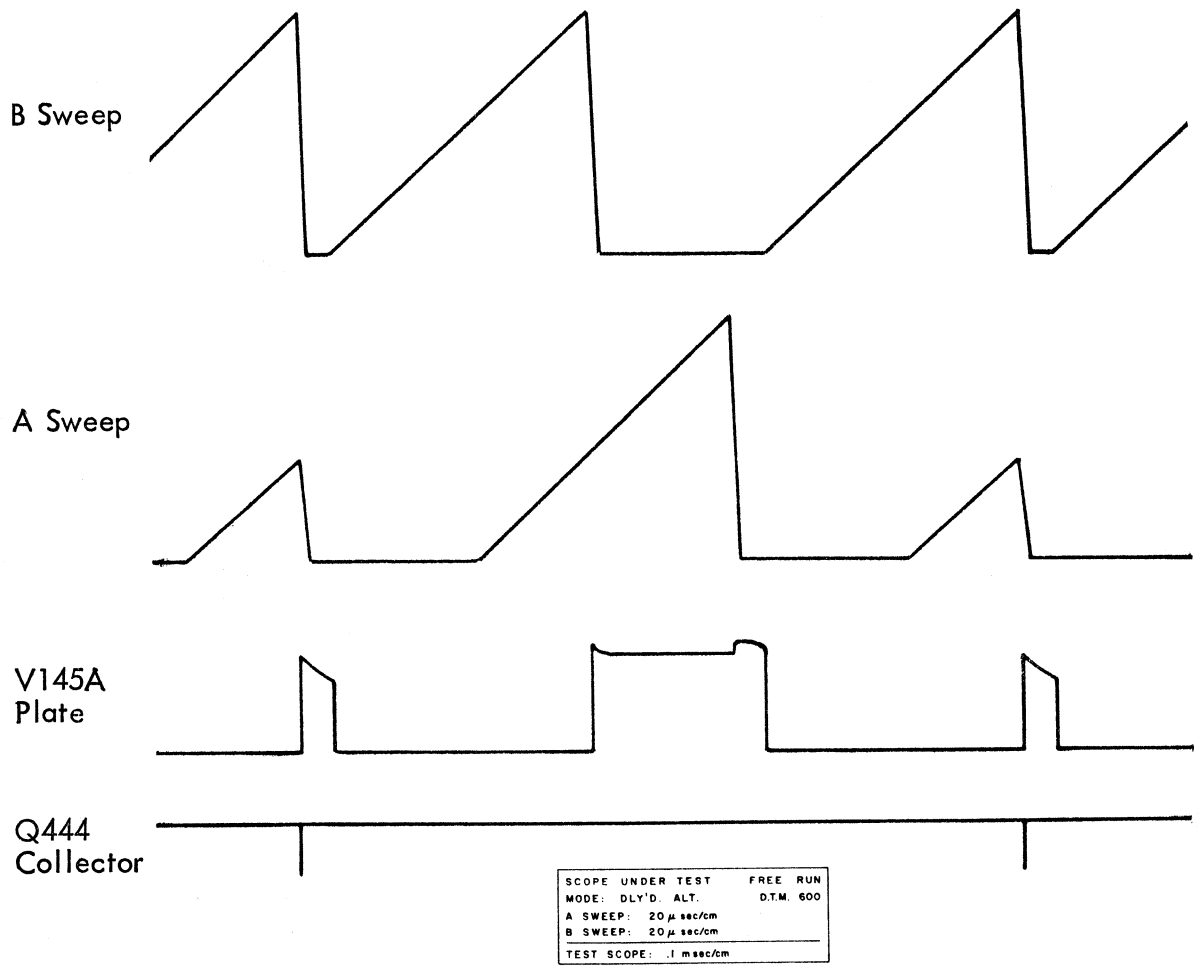
b. Should a combination of SWEEP TIME/CM and DELAY TIME MULTIPLIER set the A sweep to run beyond the end of B sweep, the circuit terminates A sweep.



TYPE 547 SWEEP SWITCHING
ANTI WRAP-AROUND AMPLIFIER

B-547-0030x
3-13-'64 dl

2. The circuit uses a transistor and three diodes.
   a. Q444 is a 151-103 selected Motorola 2N2219 silicon NPN transistor.
   b. D441 is a GE 1N3605 silicon diode.
   c. D448 is a Hughes 6075 germanium diode.
   d. D449 is a T12G germanium diode.
3. At the end of B sweep, when the Hold-Off Multi flips cutting off V145A, a positive going step is formed at V145A plate.
   a. The step (about 15v) passes through C449.
   b. If the left hand output from the Sweep Switching Multi is at 27v, the pulse appears on Q444 base.
      (1) In order for the B sweep terminating pulse to appear at Q444 base, the HORIZ DISPLAY switch must be in B INTENS BY A or ALT and the Switching Multi must be in position to open the B Sweep Gate.
      (2) Under this condition, D449 cathode is pulled up to 27v, cutting it off.
      (3) If the Multi output is at 0v, the positive going terminating pulse will pull D449 into conduction.
      (4) The pulse current will pass to ground.
   c. The step is differentiated in C449, R448.
      (1) The T_c is 39 μsec.
      (2) Amplitude about 2v.
      (3) D448 cuts off.



4. The pulse forward biases Q444 and appears across the collector load amplified and inverted.

   a. The negative going (40v) pulse passes through C441 and cuts off D441.

5. If A sweep is running up, V345B in the A sweep Hold-Off Multi will be conducting.

   a. The negative going pulse will pull down on D347 (A sweep hold-off).

   b. With V345B grid pulled negative, the Hold-Off Multi flips, terminating sweep.

6. If, at the end of B sweep, A sweep has already terminated, D347 will be cut off (V345B grid at -22v).

   a. The terminating pulse does not reach V345B grid.

7. At the end of B sweep hold-off time, when the B sweep Hold-Off Multi flips and V145A conducts, a negative step is formed on its plate.

   a. As the step passes through C449, D448 conducts and the pulse current passes to ground.

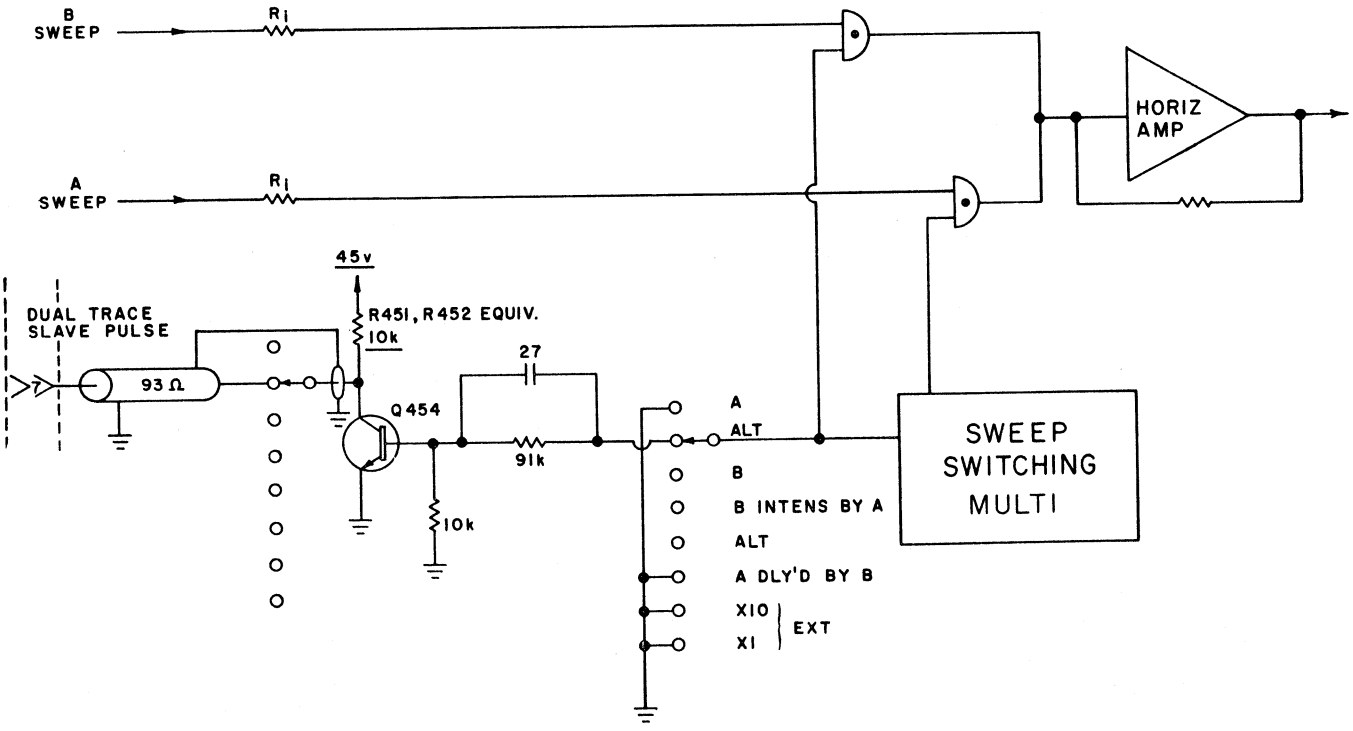
K. Dual Trace Slave Circuit

1. The circuit provides a slaving pulse to keep a dual trace plug-in in step with the Sweep Switching circuit.

   a. The pulse is fed to the plug-in via pin 7 of the blue ribbon connector.

   b. The circuit functions only in the A ALT B mode (not in the INTEN - ALT - DLY'D mode).

   c. Channel 1 (or A) will always be displayed on A sweep and Channel 2 (or B) will be displayed on B sweep.



TYPE 547 SWEEP SWITCHING
DUAL TRACE SLAVE CIRCUIT

B-547-0029x
3-11-'64 dl

2. The circuit is a one transistor DC coupled switch.

   a. Q454 is a 151-103 like Q444.

3. The base of Q454 is tied (through R454) to the left hand output of Switching Multi.

   a. When this output is at 0v (A sweep displayed), Q454 is cut off.

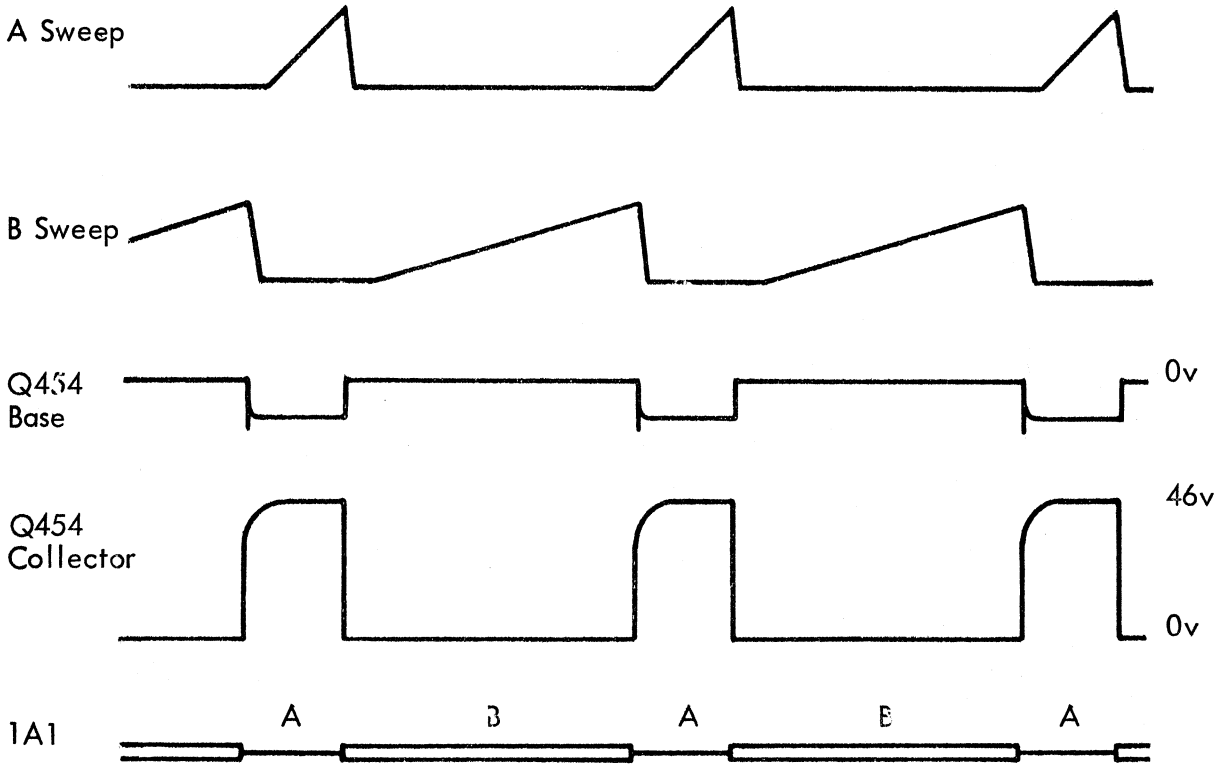
   b. Q454 collector is at 45v.

      (1) The collector load is equivalent 10k to 45v (R451, R452 equivalent).

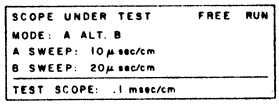
   c. When the Multi output is at 27v (B sweep displayed), Q454 saturates.

   d. The collector pulls down to ground.

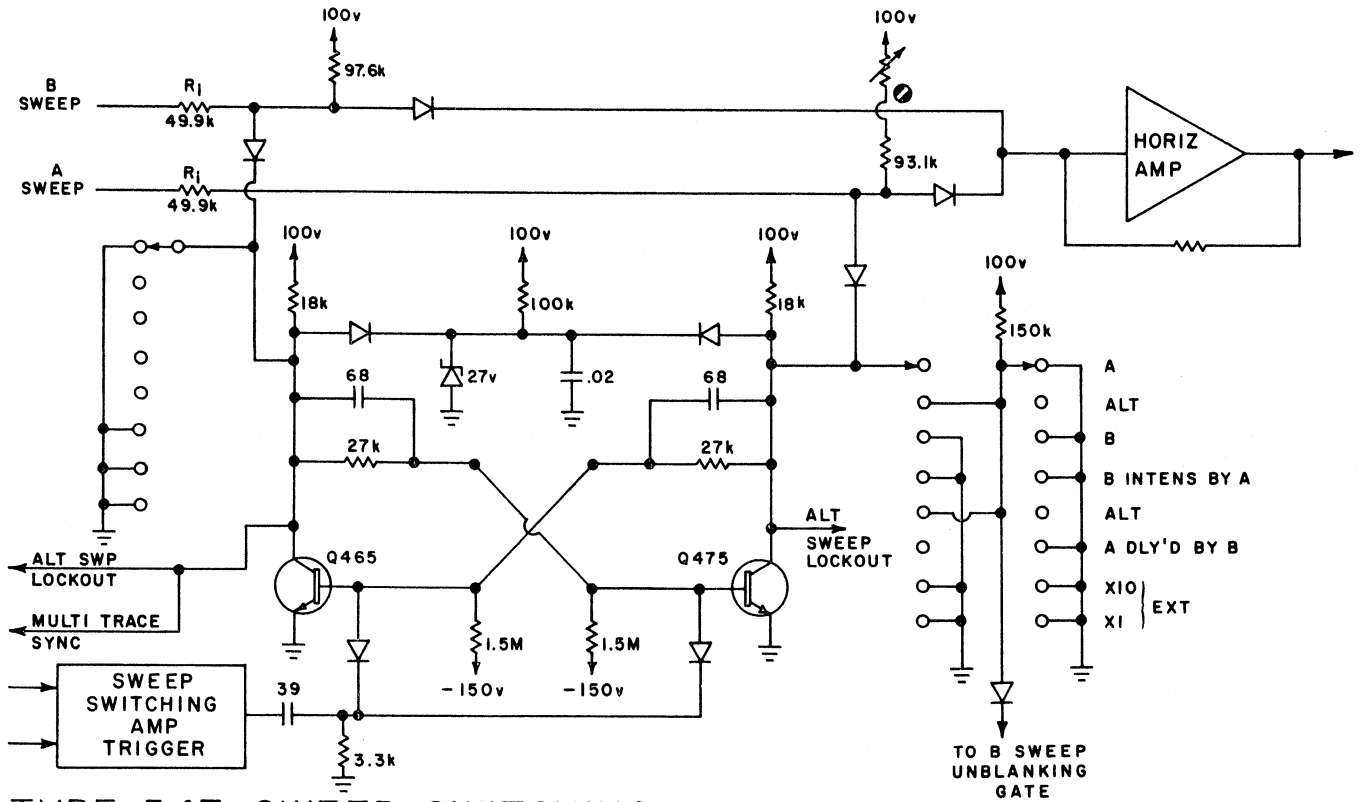
4. The circuit output at pin 7* is at 0v when B sweep is displayed and at 45v when A sweep is displayed.



* Pin 7 is grounded through the 1A1 when 1A1 is not in ALT.



L. Ancillary Functions



TYPE 547 SWEEP SWITCHING
ANCILLARY OUTPUTS

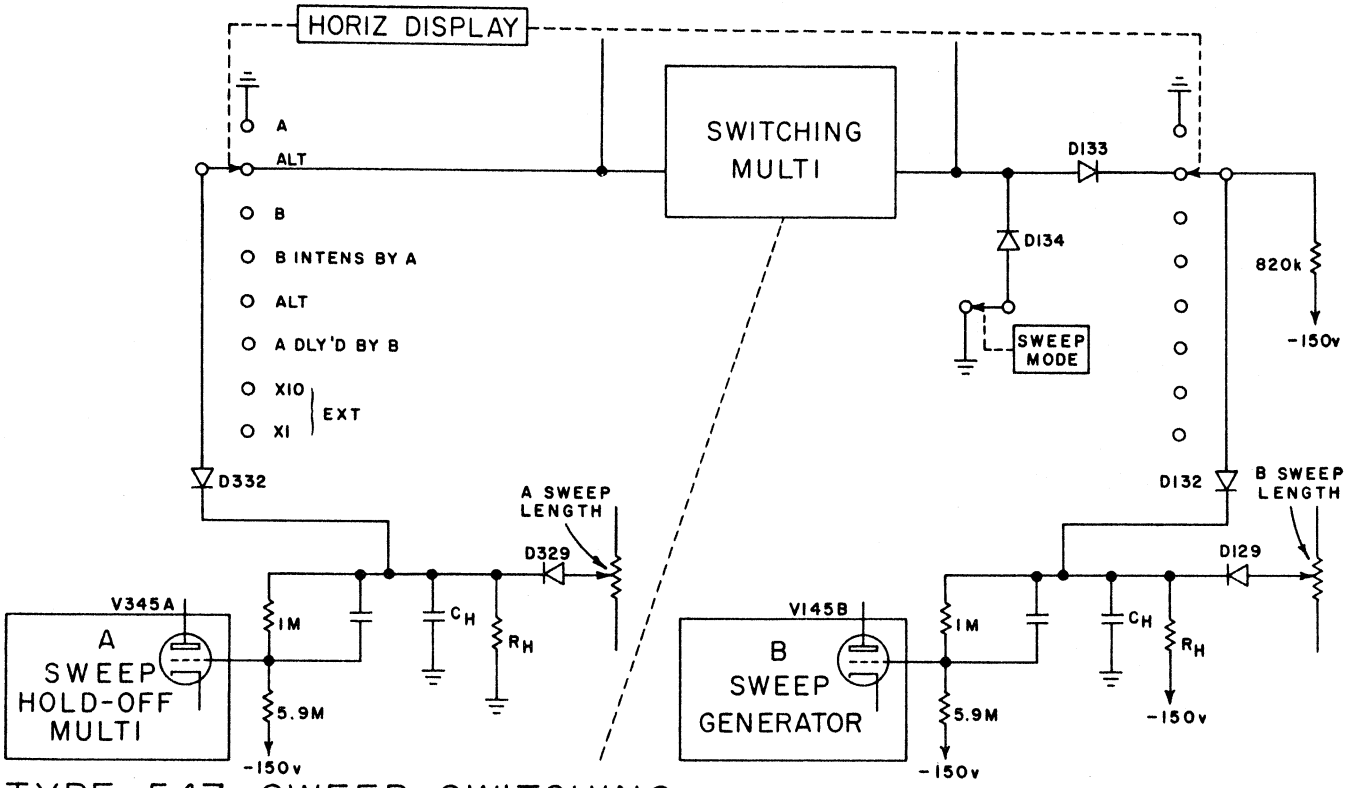
B-547-0031x
3-13-'64 dl

1. The Sweep Switching circuit supplies four additional outputs.
   a. An Alt Sweep Lockout to the A Sweep Generator.
   b. An Alt Sweep Lockout to the B Sweep Generator.
   c. A Multi-Trace Sync pulse for multi-trace switch in a Vertical Preamplifier.
   d. A waveform to operate the B Unblanking Gate.

2. Alt Sweep Lockout to A Sweep Generator.

   a. Functions only in the A-ALT-B mode.

   b. The circuit prevents A sweep from running while B sweep is being displayed.



TYPE 547 SWEEP SWITCHING LOCKOUT CIRCUIT

B-547-0032 x
3-16-'64 dl

   c. In this mode, a connection is made from Q465 collector through D332 (A sweep hold-off circuit) to the A sweep hold-off bus.

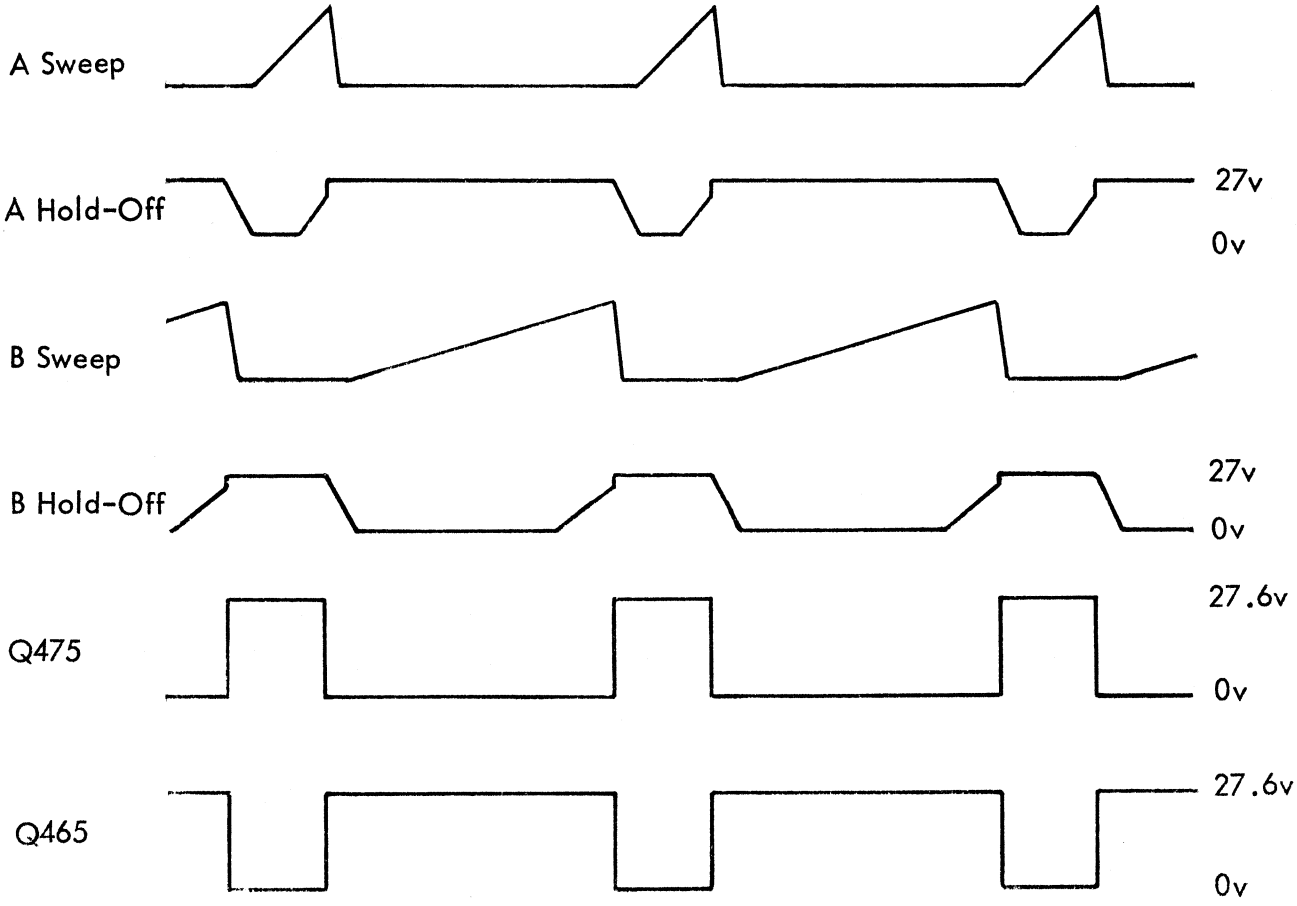
d. During the time B sweep is displayed, D332 anode is pulled up to 27v.

(1) A sweep cannot complete hold-off.

(2) A sweep circuit cannot become armed.

e. At the end of B sweep, when the Sweep Switching Multi flips, D332 anode drops to 0v.

(1) A sweep can complete hold-off.



3. Alt Sweep Lockout to B Sweep Generator.

a. The circuit prevents B sweep from running while A sweep is being displayed.

b. When A sweep is displayed, D132 (B sweep) anode is pulled up to 27v (through D133).

(1) B sweep cannot complete hold-off.

c. At the end of A sweep, the lockout voltage is removed.

(1) B sweep can complete hold-off.

4. The Multi-Trace Sync pulse provides a switching waveform for a multi-trace plug-in.

a. It functions only in the INTEN-ALT-DLY'D mode.

b. Connection is made from Q465 collector (Sweep Switching Multi) to the Multi-Trace Sync amp.

c. Only the positive going step is utilized.

d. Since a positive going step occurs only at the end of A sweep display, a dual-trace-plug-in can display both A and B sweep on each of its channels.

5. B Unblanking Gate output.

a. The waveform gates the B Sweep unblanking circuit into operation when needed.

b. The circuit operates only in the two ALT modes (it is only needed in the ALT DLY'D mode).

c. When A sweep is being displayed and Q475 collector is at 27v, D481 anode is pulled up to 27v.

(1) This positive voltage cuts off Q184 (B Sweep Unblanking).

(2) B Unblanking circuit is disabled.

d. When B sweep is displayed and Q475 collector drops to 0v, Q184 base is dropped to -.7v enabling the B Unblanking circuit.

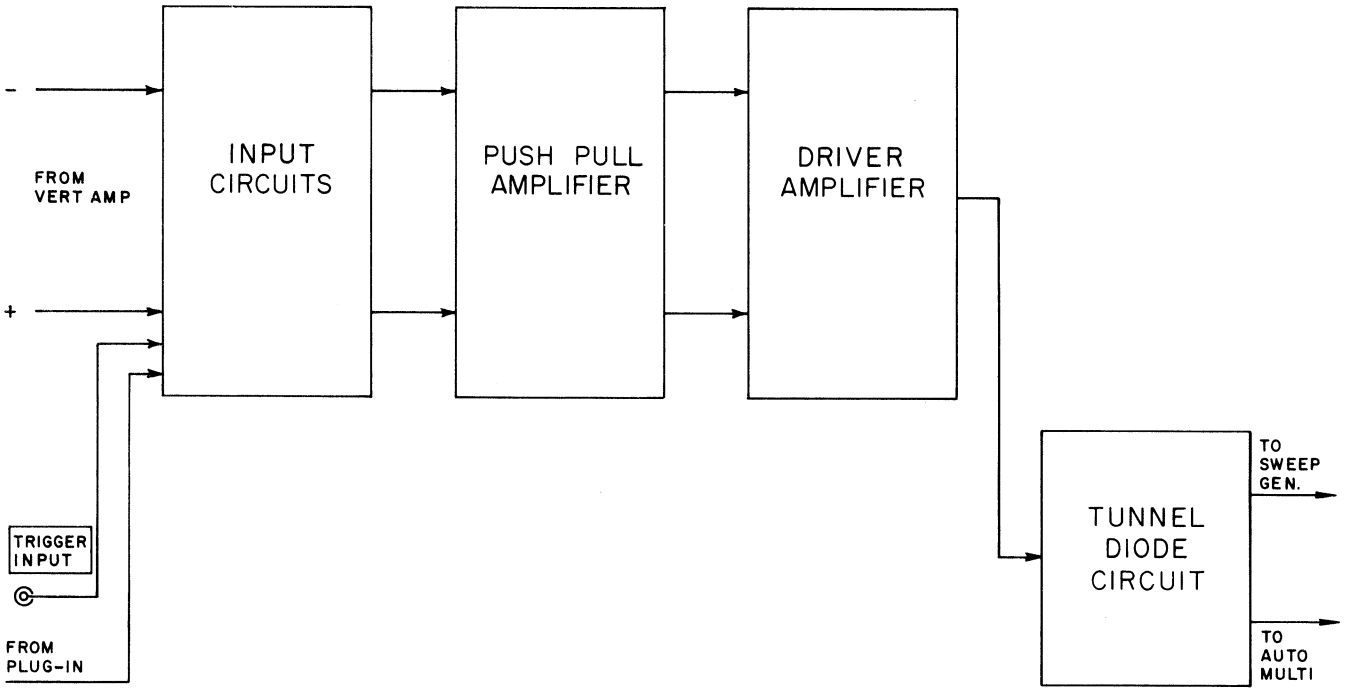
(1) B Unblanking circuit is gated on.

TYPE 547

IX. TRIGGER CIRCUITS

A. Two identical trigger circuits provide triggers to the A Sweep and B Sweep Generators.

1. This discussion will refer to the A trigger circuit.



TYPE 547 TRIGGER CIRCUITS
BLOCK DIAGRAM

B-547-0045
4-22-'64 dl

B. The circuit consists of a cathode coupled push-pull amplifier, a push-pull-to-single ended amplifier and a bistable tunnel diode.

C. The output is a 500 mv positive going pulse with a risetime of about 1/2 nsec.

D. Operating modes (selected from front panel lever wafer switches).

1. TRIGGERING SOURCE
    a. INT NORMAL
    b. INT PLUG-IN
    c. LINE
    d. EXT
2. TRIGGER COUPLING
    a. AC
    b. AC LF REJ
    c. DC
3. TRIGGERING SLOPE
    a. + or -
4. AUTOMATIC

E. INPUTS (selected by the SOURCE switch)

1. EXTERNAL (front panel jack).
    a. 1M at about 15 pf.
2. LINE
    a. About 1v RMS.
    b. The sine wave has been attenuated so the triggering level control will allow triggering at any point on the waveform.
3. PLUG-IN
    a. From pin 5 of the blue ribbon connector.

4. INTERNAL

a. A push-pull signal from the Vertical Amplifier Trigger Pick-Off.

b. About 800 mv push-pull.

F. Control

1. TRIGGERING LEVEL

a. Selects the level on the input waveform at which triggering will occur.

b. An X10 range increase switch is actuated when the TRIGGERING LEVEL knob is pulled.

c. Two ranges allow a wide dynamic range for big signals and a sensitive adjustment for smaller signals.

G. Input Circuits

1. NORM INT Mode

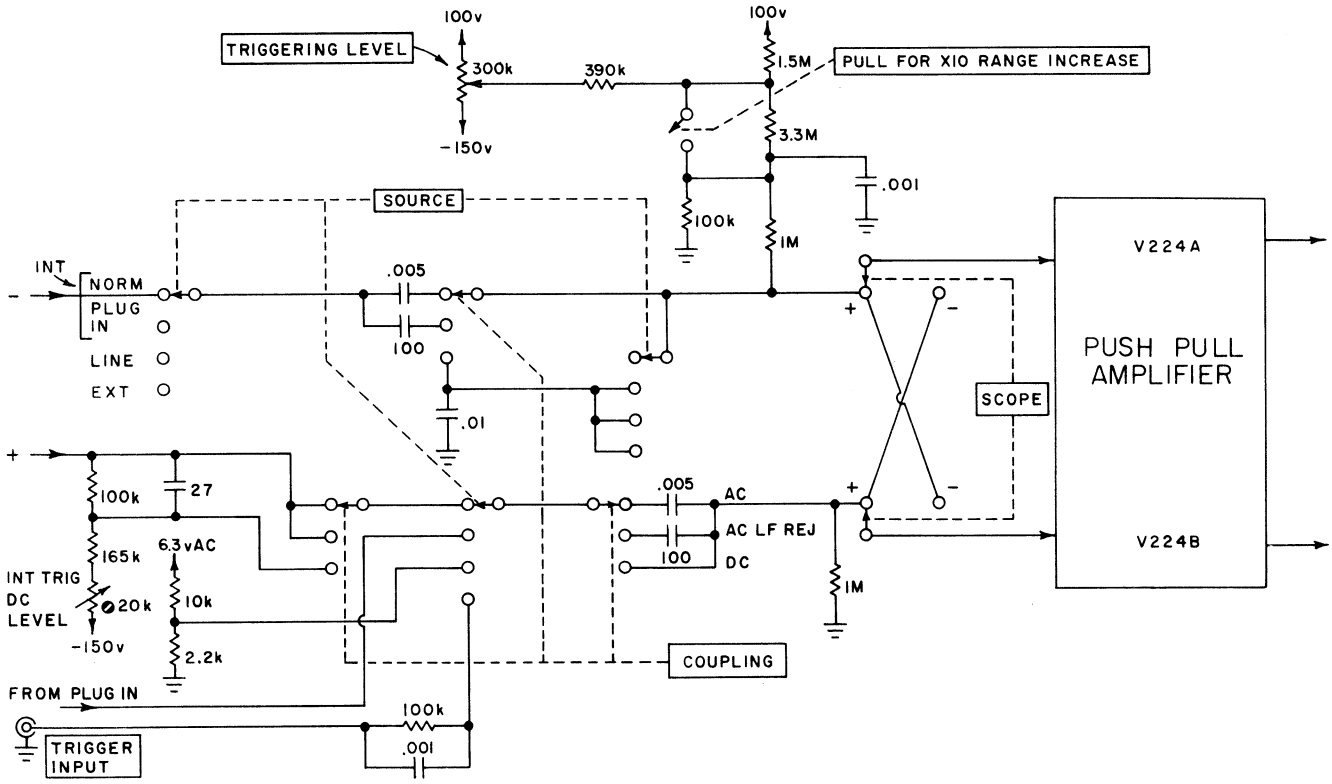
a. The input is a 700 mv to 800 mv/cm push-pull signal from the Vertical Trigger Pick-Off circuit.

b. Source impedance is 186 ohms (93 ohms each side).

c. In AC and AC LF REJ, the input is push-pull, but in DC COUPLING, the minus side is disconnected from the pick-off circuit.

(1) The push-pull input tends to reject common mode noise.

d. In the DC position of the COUPLING switch, the plus side of the input from the Vertical Amplifier is attenuated about 35% by the INT TRIG DC LEVEL divider and further effectively reduced by one-half by being a single ended signal.



TYPE 547 TRIGGER CIRCUITS
INPUT CIRCUITS

B-547-0046x
4-24-'64 dl

e. The INT TRIG DC LEVEL adjust provides a method of setting the DC level of the input signal at exactly zero volts when the trace is centered vertically.

(1) The DC level at the top of the divider is approximately 85v.

(2) A 27 pf capacitor compensates the divider.

2. PLUG-IN INT Mode

a. A single ended signal from the plug-in via pin 5 of the blue ribbon connector.

b. Signal amplitude is a minimum 500 mv/cm (typically about 900 mv/cm).

(1) Directly in parallel with CH 1 TRIGGER out jack on a 1A1.

c. Makes it possible to trigger internally from one channel of a multi channel plug-in.

3. LINE Mode

a. 6.3v AC is attenuated to about 1v RMS.

b. The AC sine wave is applied to the plus side of the trigger amplifiers.

c. DC coupling is available as well as AC and AC LF REJ.

4. EXT Mode

a. Tied to the front panel TRIGGER INPUT jack (BNC).

b. A 100k protective resistor is provided, bypassed by a .001 μf capacitor.

c. Input impedance is 1M at about 15 pf (B TRIGGER INPUT is about 20 pf).

d. Will trigger on 200 mv.

5. Coupling Switch

   a. The AC position places a .005 μf in both sides of the feed from the Vertical Amplifier in the NORM INT mode.

      (1) Trigger input is 3 db down at about 30 cps.

      (2) T_C is 5 msec.

   b. The AC LF REJ position places a 100 pf capacitor in both sides of the NORM INT input.

      (1) 3 db down at about 1.4 kc.

      (2) T_C is 100 μsec.

   c. The DC position of the switch opens the minus side of the feed from the Vertical Amplifier.

      (1) The positive side is connected through a 100k resistor to the Vertical Amplifier Trigger Take-Off Circuit.

      (2) The DC level is set at 0v (trace centered vertically) by the INT TRIG DC LEVEL adj.

6. TRIGGERING LEVEL Control

   a. Has a normal range (knob pushed in) of about ±2.5v at V224 grid.

      (1) Meter loading may give erroneous reading.

   b. X10 range increase (knob pulled out) increases the range to ±25v.

   c. Sets the DC level on V224A grid (or V224B grid when in - SLOPE).

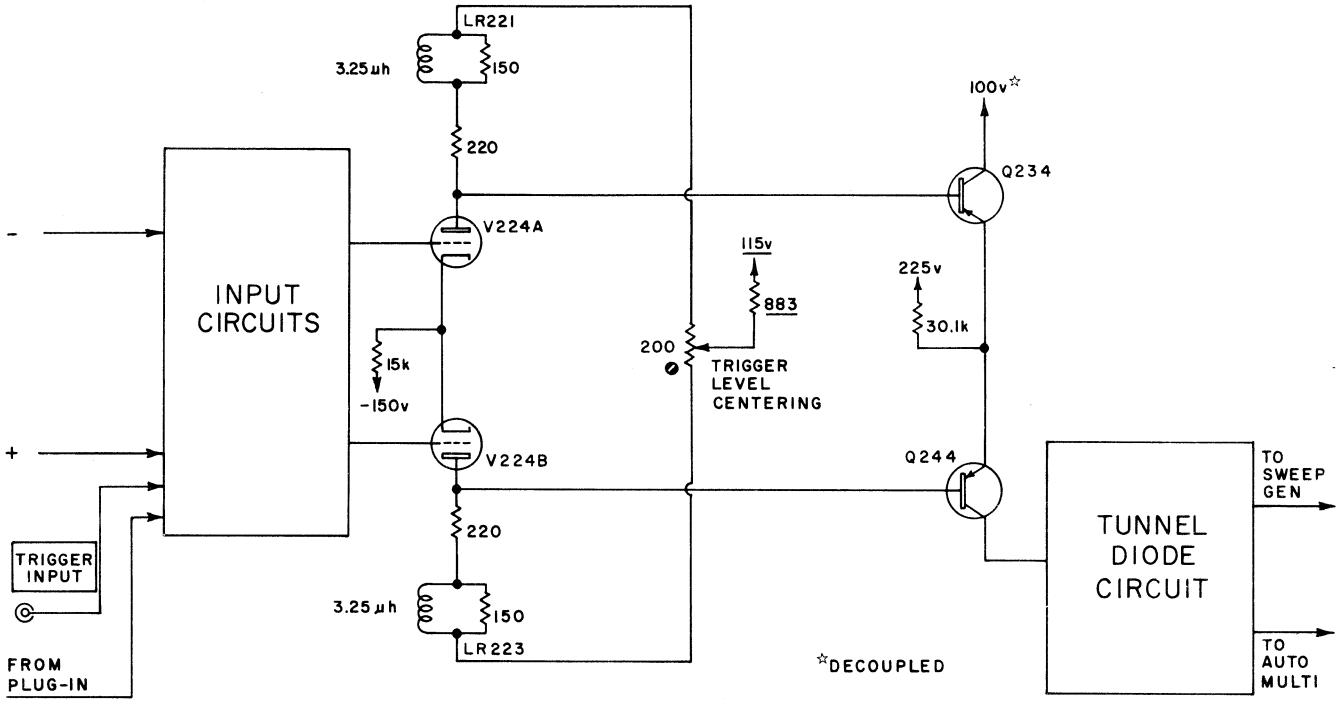
7. SLOPE Switch

   a. Reverses the polarity of the input signal.

   b. Connection to V224A and V224B grids is reversed.

   c. In DC position in INT NORM mode and in PLUG-IN, LINE and EXT, the signal can be switched to V224A grid instead of V224B grid.

H. Push-Pull Amplifier



TYPE 547 TRIGGER CIRCUITS
PUSH PULL AMPLIFIER AND DRIVER AMPLIFIER

B-547-0047x
4-24-'64 dl

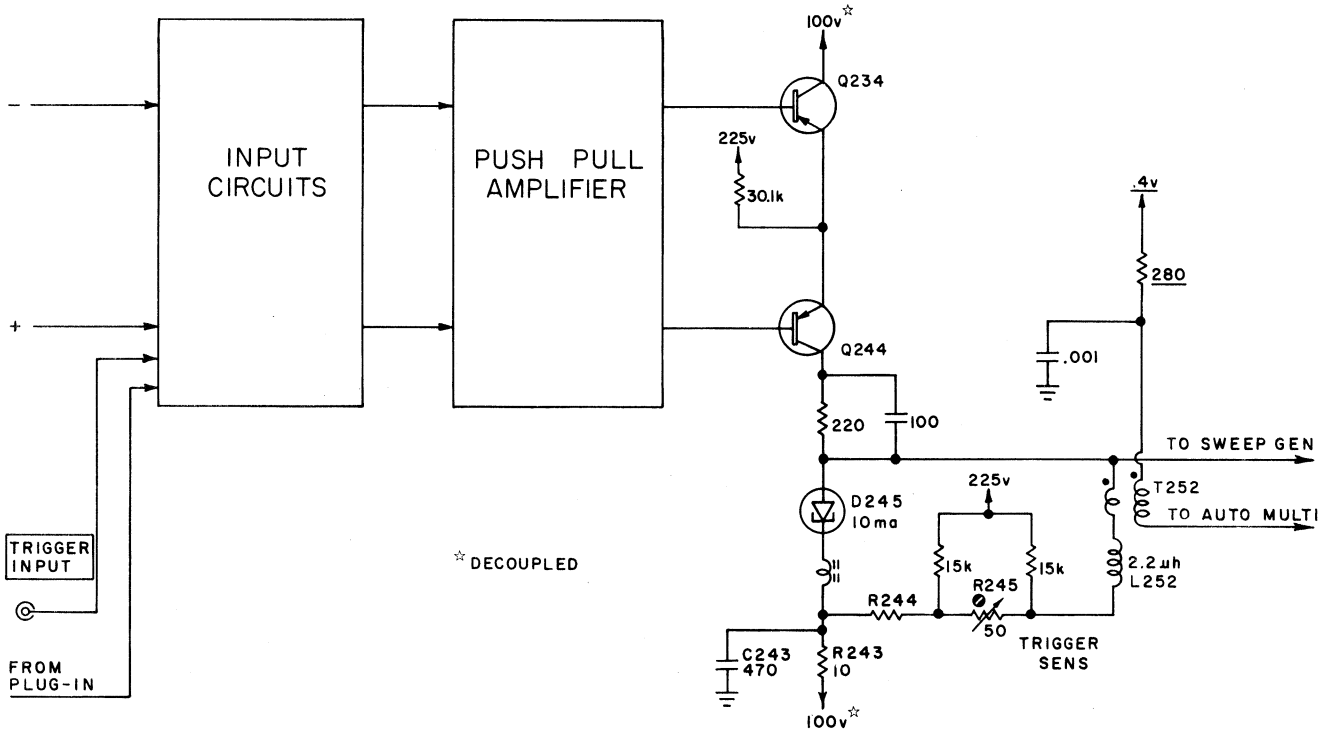
1. The amplifier uses two halves of a 6DJ8 dual triode.
   a. Vacuum tubes make high input Z (EXT mode) practical.
2. When a push-pull signal is received (NORM INT mode with AC or AC LF REJ coupling), the circuit is a cathode coupled push-pull amplifier.
3. When a single ended signal is used, the circuit becomes a paraphase inverter.
4. The circuit can be considered a differential amplifier. The circuit measures the difference voltage between the grids.
   a. The TRIGGERING LEVEL control can swing the grids as much as ±25v (X10 RANGE INCREASE).
   b. The long-tail cathodes allow the grids to work at these levels with little change in plate current.
5. The amplifier has a voltage gain of about 2.
   a. The output has a swing of about 1.4 v/cm push-pull.
6. Low value plate load resistors and peaking networks, LR221 and LR223, assure fast response to a fast trigger.
7. Plate current is supplied through the TRIGGER LEVEL CENTERING control and an equivalent 883Ω to 115v.
8. The TRIGGER LEVEL CENTERING control sets the current through Q224 in the middle of the tunnel diode hysteresis range for either + or - slope.
   a. A screwdriver calibration adjustment.
   b. Normally, the adjustment will set equal currents through Q234 and Q244.

I. Driver Amplifier

1. The Driver Amplifier is an emitter coupled push-pull to single ended amplifier.
    a. Q234 and Q244 are Motorola 2N962 germanium PNP transistors.
2. The triggering waveform switches current from one transistor to the other.
3. The emitters are long-tailed to 225v.
    a. They set at 103v.
    b. Quiescently, about 2 ma flows through each transistor.
4. As current in Q244 increases, the TD flips to its high state starting sweep.

J. Tunnel Diode Circuit

1. The Tunnel Diode circuit provides a triggering pulse of uniform amplitude and shape regardless of the shape of the input trigger.



TYPE 547 TRIGGER CIRCUITS
TUNNEL DIODE CIRCUIT

B-547-0048x
4-27-'64 dl

2. The circuit uses a GE TD-253 10 ma tunnel diode.

3. Choice of tunnel diode load resistance places the TD in a bistable configuration.

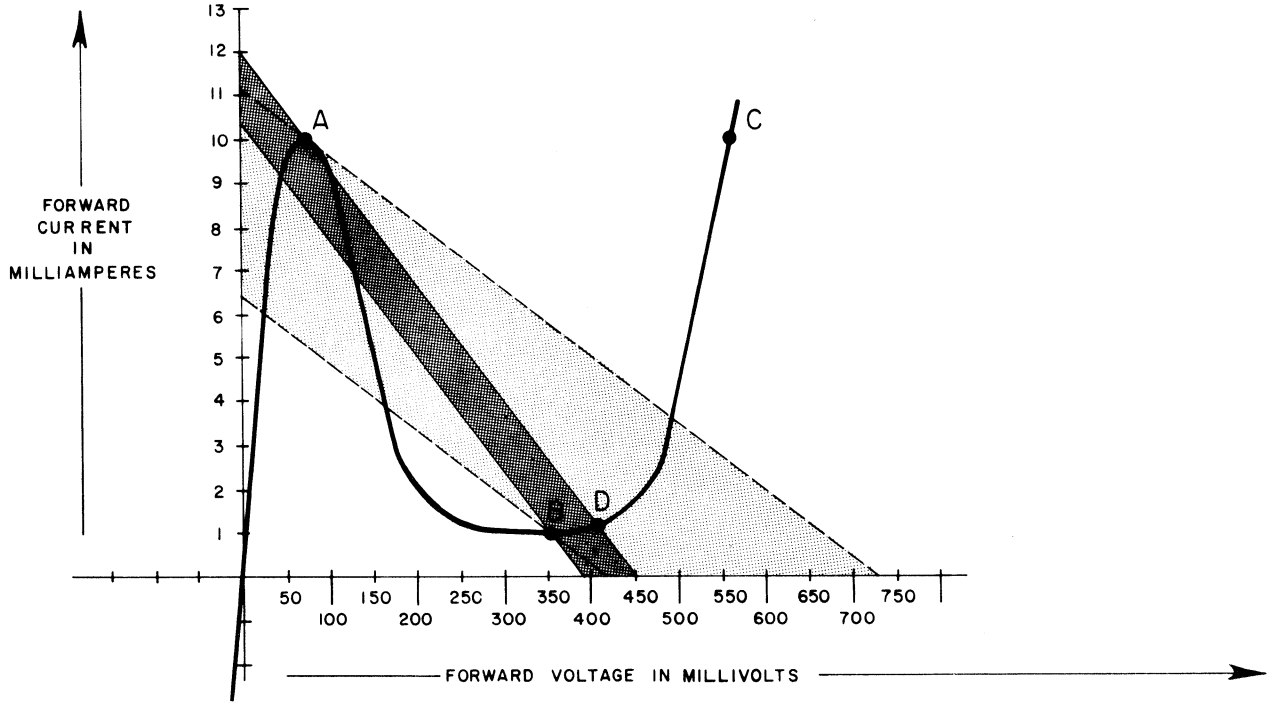
   a. R44 and R45 constitute the TD load.

4. A bistable tunnel diode has <u>current</u> hysteresis.

   a. The width of the hysteresis gap is determined by the TD load.

   b. The load resistance and, therefore, the width of the hysteresis gap can be controlled by the TRIGGER SENSITIVITY control.

5. Tunnel diode curve:



   a. The limits of the hysteresis gap can be represented by the load lines.

      (1) The top of the hysteresis gap (point A) appears in the TD low voltage state.

      (2) The bottom of the gap (poing B) appears in the high state.

b. The slope of the load lines determines the width of the hysteresis gap.

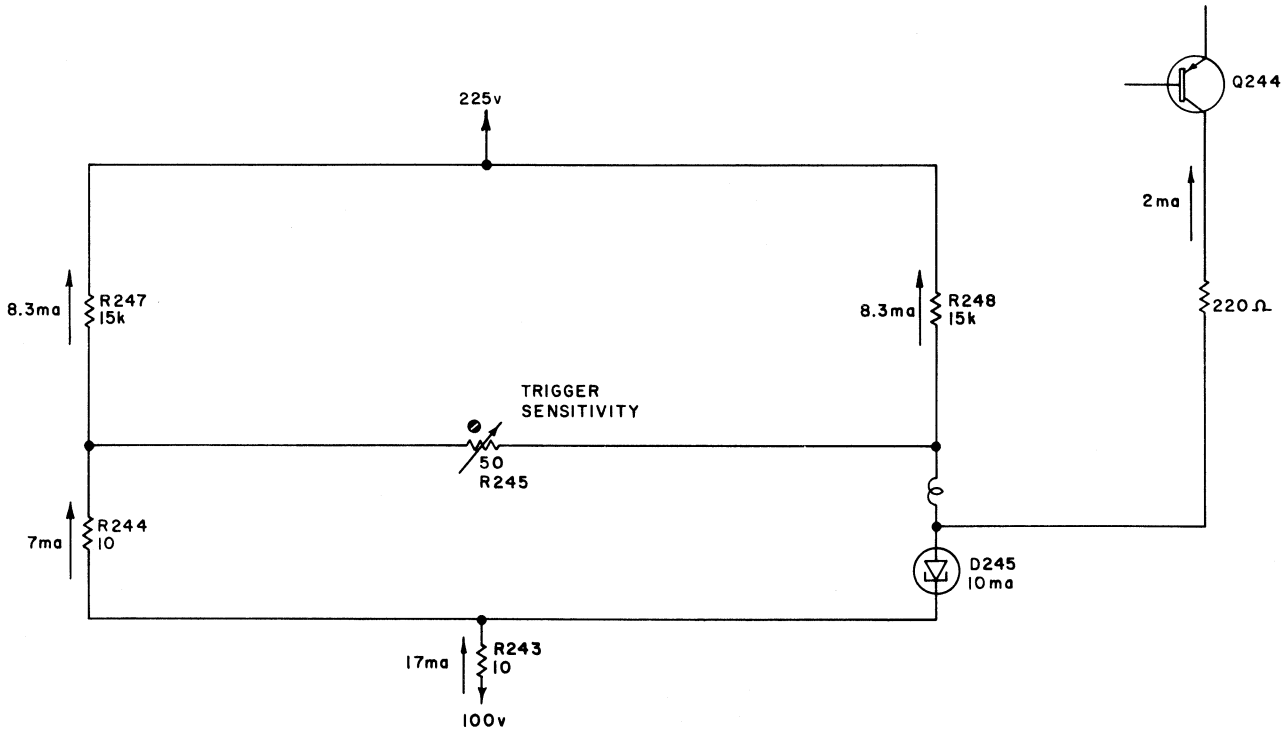
(1) The setting of the TRIGGER SENSITIVITY control sets the slope of the load lines.

(2) The less the resistance, the steeper the slope.

c. The darker shaded area represents a relatively sensitive setting of the TRIGGER SENSITIVITY control (narrow hysteresis gap).

d. The lighter shaded area represents a relatively insensitive setting (wide hysteresis gap).

6. Current Distribution:



TYPE 547 TRIGGER CIRCUITS
T. D. CURRENT DISTRIBUTION

B-547-0049x
4-27-'64 dl

a. Q244 can draw from 0 to 4 ma from the TD circuit.

b. The current through R244 depends on whether the TD is in its low or high state.

c. About 7 ma flows through R244 when the TD is in its low state and about 17 ma in its high state.

d. The TD must draw at least 10 ma to flip it to its high state and less than 1 ma to flip it to its low state.

7. Assume the TD is in its low state awaiting a trigger.

a. The triggering waveform biases Q244 to greater conduction.

b. Increased current through the TD flips it to its high state.

(1) L252 presents a high impedance load momentarily and the TD flips to point C.

(2) The load line, as the TD switches, is essentially flat.

c. If the triggering waveform is a fast pulse, the TD flips back to its low state.

(1) The change from point C to point B on the TD curve is slowed by L252.

(2) This provides a count-down at high frequencies.

(3) Count-down begins at 1-5 mc on small signals and up to 10 mc on large signals.

d. If the triggering waveform is a long duration waveform, the TD will rest at point D for the duration of the waveform.

(1) When the TD flipped to its high state, current in R44 increased, leaving only 1.5 ma flowing through the TD.

(2) At the end of the waveform, current through Q244 decreases; the TD current drops below 1 ma and flips to its low state.

e. The circuit has returned to its quiescent state.

8. The output waveform is taken across the TD.

a. As the TD flips to its high state, the voltage appears across T252 primary as a step about 500 mv in amplitude.

b. The voltage drop across the TD raises to 560 mv (from 75 mv), then as L252 allows current to flow in the load resistance, the TD drops to point D.

(1) . The result is a 100 mv overshoot.

c. The step (and overshoot) is differentiated in the Sweep Generator circuit.

(1) The result is a 2 nsec pulse with a risetime of a 1/2 nsec.

9. T252 secondary feeds the AUTO multi.

a. The waveform at T252 secondary is a negative going .8v pulse of about 700 nsec duration with about 40 nsec risetime.

10. L244 is a ferrite bead that keeps fast transients from flipping the TD.

11. R243 and C243 provide additional decoupling.

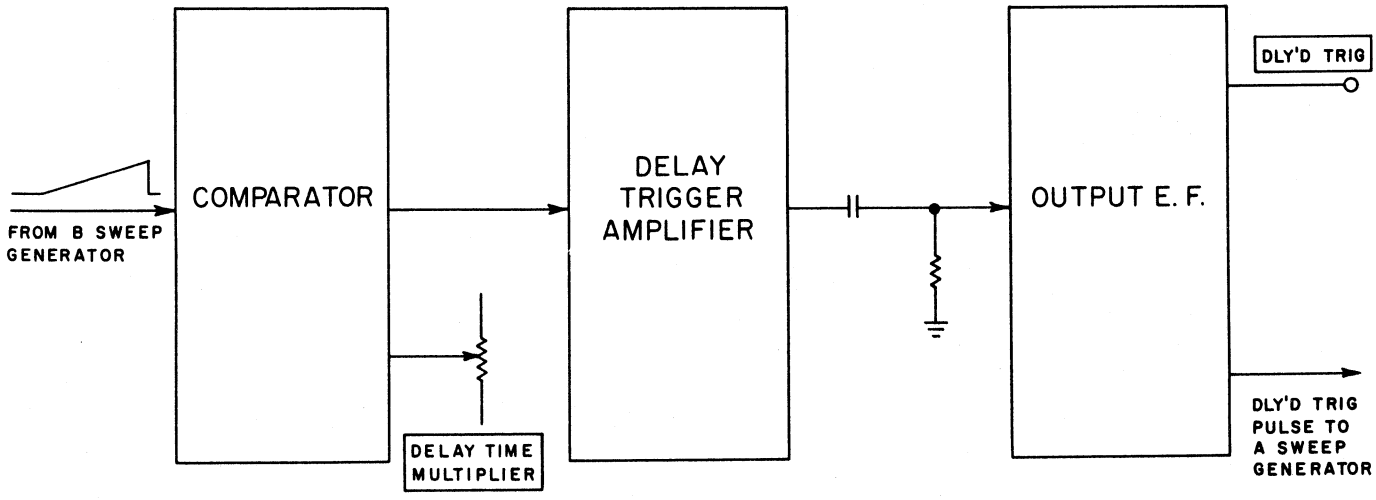
TYPE 547

X. DELAY PICKOFF

A. The Delay Pickoff provides a delayed trigger pulse to the A Sweep Generator.

1. The delay time is calibrated.
2. An EXT DLY'D TRIG is available at a front panel jack in all HORIZONTAL DISPLAY modes.
3. The delayed trigger pulse is fed to the A Sweep Generator only in the B INTENS BY A, A DLY'D BY B, and the INTENS-ALT-DLY'D modes.

B. Block Diagram



TYPE 547 DELAY PICKOFF
BLOCK DIAGRAM

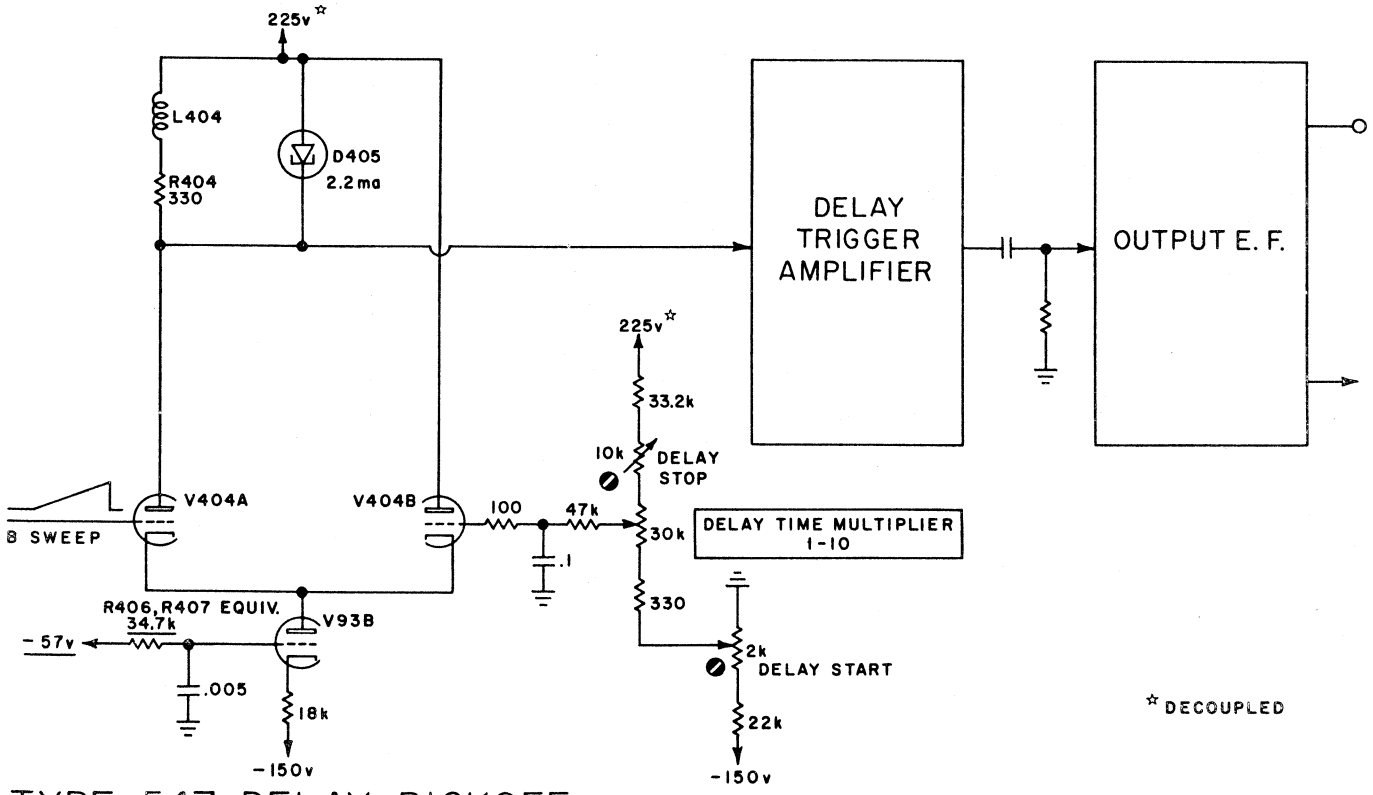
B-547-0033
3-16-'64 dl

C. Block Logic

1. The 100v sawtooth from the B Sweep Generator is fed to the comparator circuit.
2. After a delay controlled by the DELAY TIME MULTIPLIER, a 500 mv negative step appears at the comparator output.
3. The step is amplified and inverted and differentiated in the Delay Trigger Amplifier.
4. The positive going pulse out of the Delay Trigger Amplifier is about 15v peak-to-peak.
5. Further sharpened in the coupling network, the positive going pulse is delivered to the A Sweep Generator via the Output EF.

D. Comparator*

1. The comparator provides a negative going step delayed a calibrated time after the start of B Sweep.



TYPE 547 DELAY PICKOFF COMPARATOR

B-547-0034x
3-17-'64 dl

* Typical Oscilloscope Circuitry, page 7-6

2. The circuit uses three triodes and a tunnel diode.
   a. V404A and V404B are two halves of a 6DJ8.
   b. V93B is half of a 6DJ8 (the other half is the B sweep generator run-up CF).
   c. D405 is a GE TD202 2.2 ma tunnel diode (an epoxy encapsulated TD-2A).
3. The positive going 100v B sweep is applied to V404A grid.
   a. The B sweep ramp starts at about -2v.
   b. Depending on sweep length and sweep speed, the ramp amplitude will vary from 110v (10.5cm) to 135v at fast sweep speeds.
4. The DELAY TIME MULTIPLIER sets the level on V404B grid.
   a. The DELAY TIME MULTIPLIER is a 10 turn Helipot with a resistance of 30k.
      (1) Resistance tolerance is ±3%.
      (2) Linearity is ±.1%.
   b. Properly calibrated, the control has a range of from -2v to 100v.
      (1) DELAY START adjust can vary the start from -5v to +1v.
      (2) DELAY STOP can vary the stop from 93v to 107v.
      (3) There is some interaction between DELAY START and DELAY STOP adjust.

5. The constant current tube, V93B, limits the range of current through V404 as the ramp runs up.
   a. Current varies from 5.17 ma at the start of the ramp to 5.4 ma at the ramps maximum excursion.
      (1) With a 30k resistor in place of V93B, current would vary from 5 ma to 8.3 ma.
   b. The constant current improves Delay Time timing.
   c. V93B grid sets at -57v.
      (1) R406, R407 equivalent is 34.7k to -57v.
6. Prior to sweep, V404A is cut off.
7. About 2 μa of Q424 base current flows through the TD and R404, reverse biasing the TD.
   a. The TD is in its low state.
8. With the DELAY TIME MULTIPLIER set at mid range (50v), for example, the input ramp must reach 49v before V404A begins to conduct.
   a. As the ramp runs up, about 5 ma transfers from V404B to V404A.
   b. Since there is no feedback in the circuit, the current transfer is not instantaneous.
   c. As the current through D405 reaches 2.2 ma, however, the TD flips to its high state.
   d. R404 and L404 reduce the hysteresis of the TD.
   e. L404 improves the amplitude of the switching spike.

9. When the TD flips, a 500 mv negative going step drives the Delay Trigger Amplifier.

10. The TD gets a little extra boost at fast sweep speeds and the risetime of the step is improved.

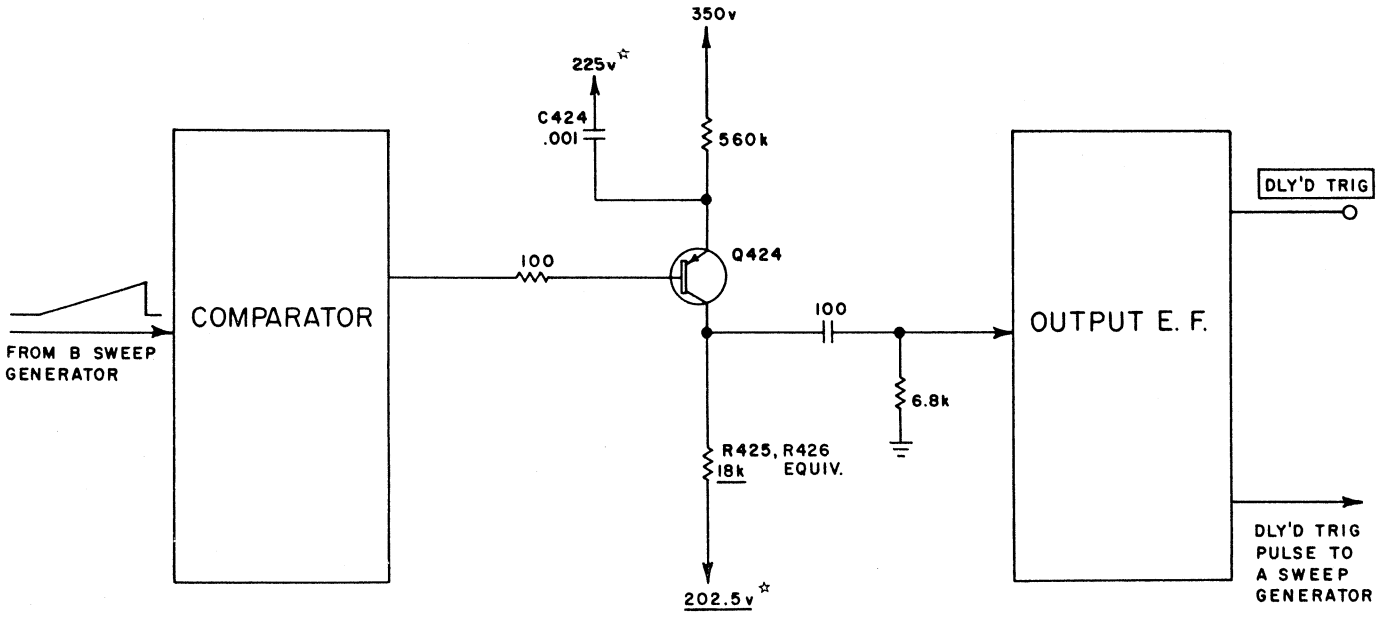
    a. The shorter risetime results in a greater amplitude trigger after the step has been differentiated.

11. At retrace, current switches back to V404B.

    a. The TD returns to its low state.

E. Delay Trigger Amplifier

1. The Delay Trigger Amplifier amplifies and differentiates the negative going step from the TD.



TYPE 547 DELAY PICKOFF
DELAY TRIGGER AMPLIFIER

B-547-0035 x
3-17-'64 dl

2. Q424 is a 2N2207 germanium PNP transistor.

3. In the quiescent state, the transistor is conducting about 250 μa.

   a. Base and emitter set at about 225v.

   b. The collector is pulled up to 207v.

      (1) Collector load is equivalent 18k to 202.5v (R426, R425 equivalent).

4. The 500 mv negative going step from the comparator drops Q424 base, increasing its forward bias.

   a. The emitter is held momentarily by the charge on C424.

   b. The collector raises about 15v.

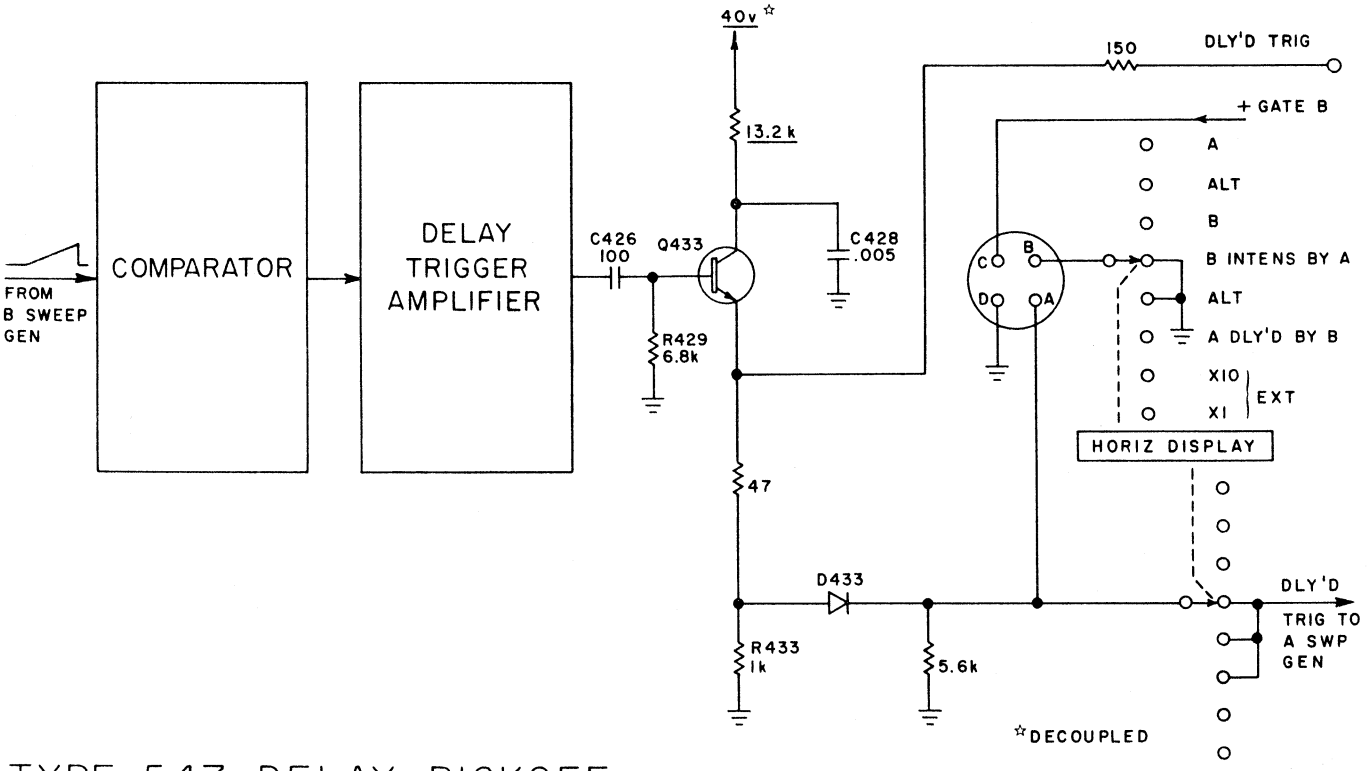
   c. As the charge on C424 leaks off, emitter degeneration reduces the amplifier gain.

   d. The collector drops back to 207v.

   e. The result is a 15v positive going pulse with a duration of 150 nsec.

F. Output Emitter Follower

1. The Output EF provides a low impedance drive to the DLY'D TRIG jack, the HORIZ DISPLAY switch and the EXT DELAY INPUT jack.



TYPE 547 DELAY PICKOFF
OUTPUT EMITTER FOLLOWER

B-547-0036x
3-19-'64 dl

2. Q433 is a 151-103 selected Motorola 2N2219 silicon NPN transistor.

3. In the quiescent state, Q433 is cut off.

   a. Both base and emitter are at ground.

   b. The collector load is equivalent 13.2k to 40v.

4. The 15v positive going trigger is further differentiated in C426, R429.

   a. The duration is reduced to about 100 nsec.

5. As the trigger pulls Q433 into conduction, C428 bypasses the collector for the duration of the pulse.

6. The negative pulse delivered to Q433 base at retrace time cannot pass the cut-off transistor.

7. The output positive going trigger is formed across R433.

   a. The trigger appears at the DLY'D TRIG jack on the scope front panel.

   b. The pulse pulls D433 into conduction and is conducted to the A Sweep Generator.

      (1) Provided the HORIZ DISPLAY switch is in the B INTENS BY A, INTEN-ALT-DLY'D, or A DLY'D BY B modes.

   c. The pulse is also present on pin A of the EXTERNAL DELAY INPUT jack.

8. The output pulse will vary from about 10v peak-to-peak at slow sweep speeds to 15v at faster speeds.

9. Output impedance is about 250 ohms.

G. EXTERNAL DELAY INPUT Jack

1. The rear panel jack provides a means of inserting an external delay trigger.

2. The B Gate is tied to pin C of the jack.

   a. The B Gate can be used as a reference for an external delay device.

3. An external positive going delayed trigger disconnects D433 and is fed to the A Sweep Generator.

4. Pin B grounds through the HORIZ DISPLAY switch in the B INTENS BY A and INTEN-ALT-DLY'D modes.

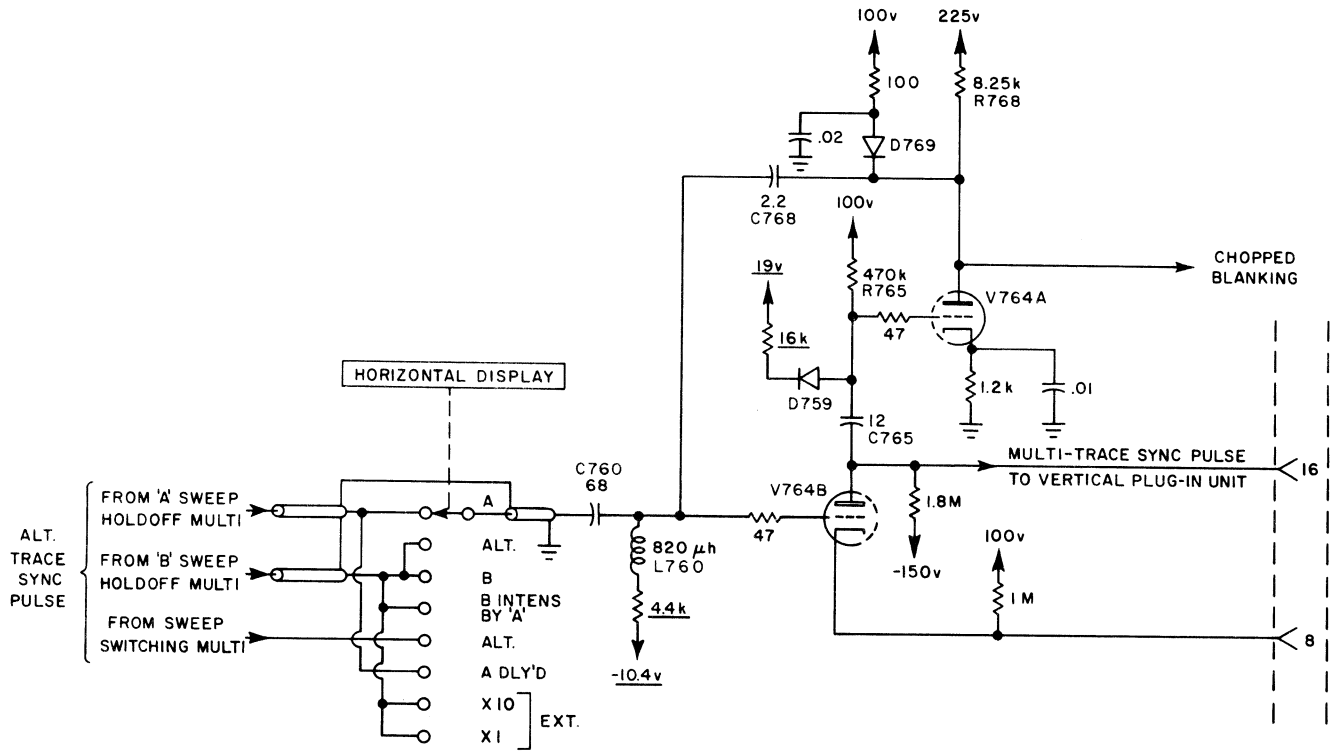
TYPE 547

XI. MULTI TRACE SYNC AMPLIFIER

A. The Multi Trace Sync Amplifier provides a sync pulse at the end of each trace to flip the electronic switch in a Multi-Trace plug-in.

1. The pulse appears at pin 8 of the blue ribbon connector as a positive going pulse with a 1A1 (pin 16 with a CA).

2. A chopped blanking pulse is provided to blank the CRT while multi trace chopped switching spikes are present.



TYPE 547
MULTI-TRACE SYNC AMPLIFIER

B-547-0083x
4-20-'64 ms

B. Three inputs drive the Sync Amp.

1. From A Sweep Hold-Off Multi.

a. A positive going step from the plate of V345B.

b. Connected by the Horizontal Display switch in A and in A DLY'D BY B modes.

2. From B Sweep Generator Hold-Off Multi.

a. A positive going step from the plate of V145A.

b. Connected by the Horizontal Display switch in A-ALT-B, B INTENS BY A, and EXT modes.

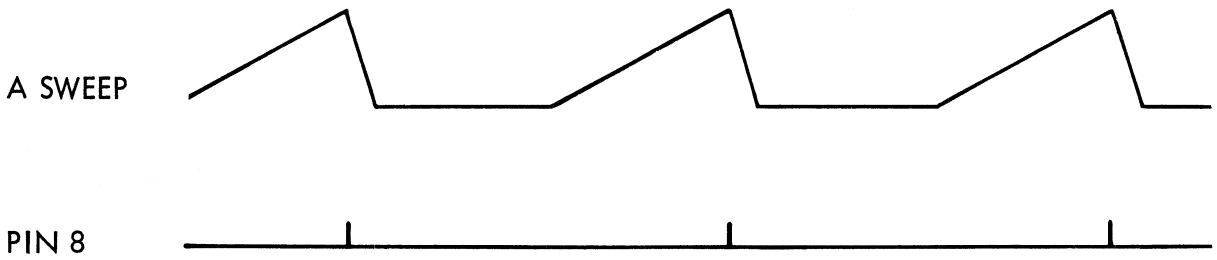
3. From the Sweep Switching Multi.

a. A positive going step from Q465 collector.

b. Connected in the DLY'D ALT mode of the Horizontal Display switch.

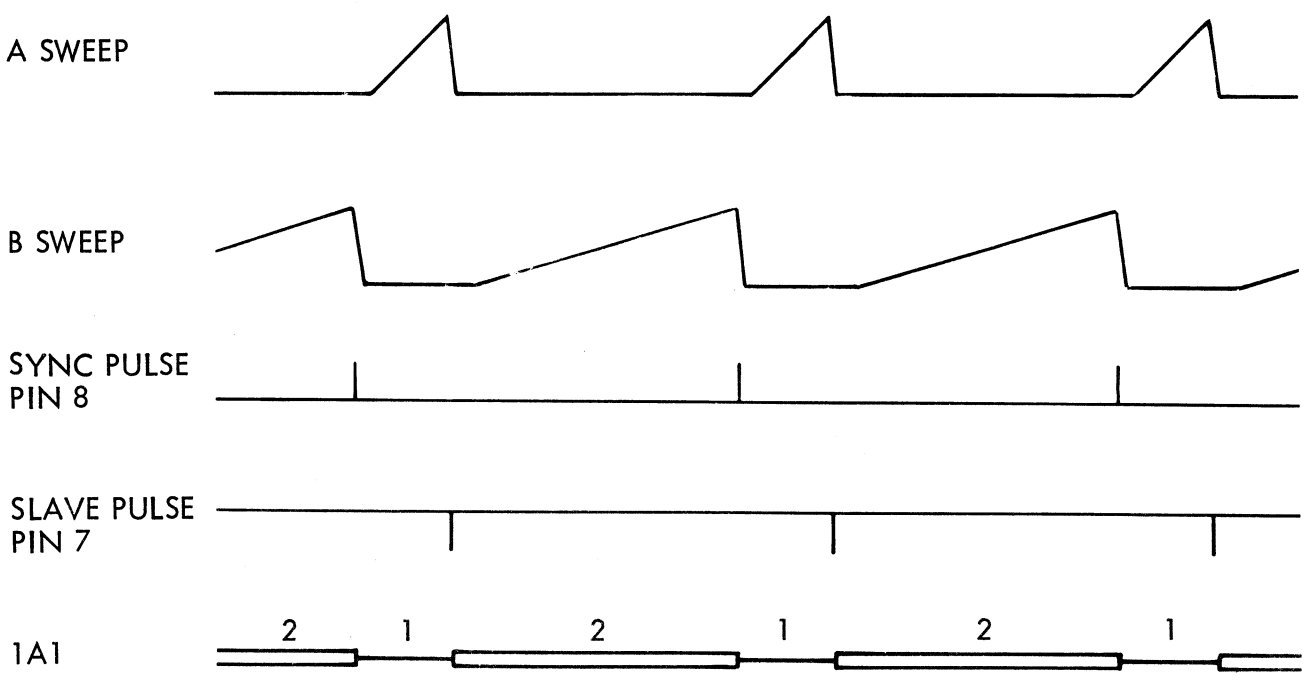
C. Multi Trace Switching Logic

1. In the A mode of the Horizontal Display switch, the multi-trace plug-in switches at the end of A sweep.



2. In the B mode, the multi-trace plug-in switches at the end of B sweep.

3. In the A-ALT-B mode, the plug-in switches at the end of B Sweep.



a. A slave pulse from the Sweep Switching circuit, through pin 7 of the blue ribbon connector, switches the plug-in at the end of A trace.

b. At the end of B Sweep, a positive going step from the B Hold-Off Multi switches the plug-in to Channel A.

c. At the end of A Sweep, a negative going step from Q454 collector (Sweep Switching circuit) switches the plug-in to B Channel.

d. Plug-in preamp Channel A will always be displayed with A Sweep and Channel B with B Sweep in this mode.

4. In the B INTENS BY A mode the plug-in switches at the end of B Sweep.

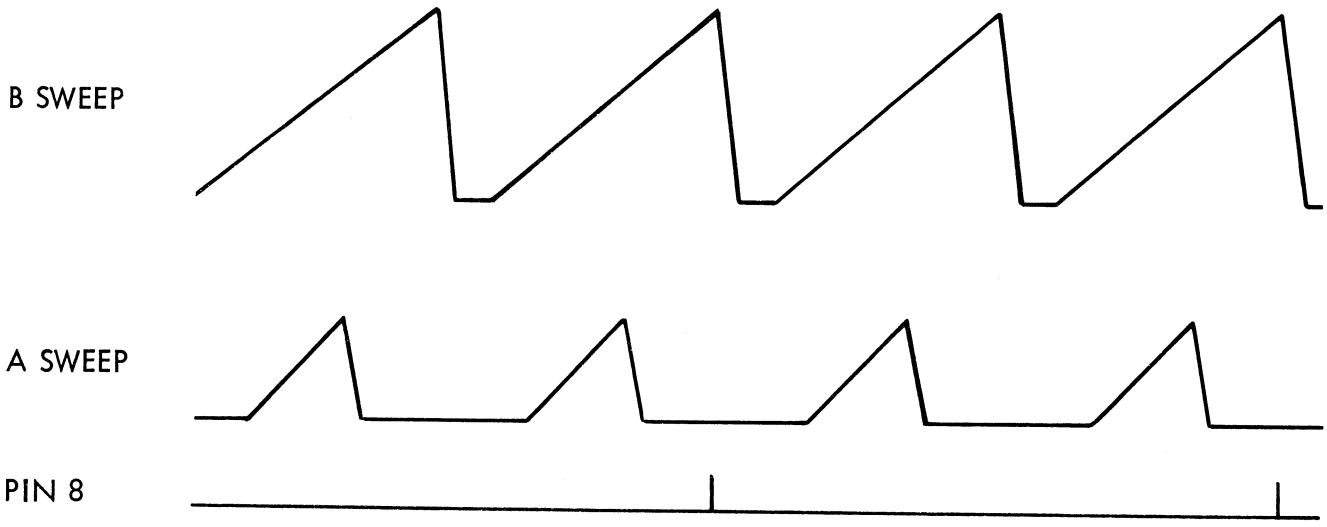
5. In A DLY'D BY B mode, the plug-in switches at the end of A Sweep.

6. In the DLY'D ALT mode, the plug-in switches at the end of every other sweep.

a. Plug-in Channel A, for example, is displayed by B Sweep as B DLY'D BY A, then by A Sweep as A INTENS BY B.

b. The plug-in then switches and B Channel is displayed alternately by both sweeps.

c. Four traces are displayed.



C. Sync Amplifier

1. The Sync Amplifier uses one-half a 6DJ8 dual triode.
2. When a Multi-Trace plug-in is not in use or when a Multi-Trace plug-in is in other than its ALT mode, the cathode is tied through 1M to +100v and the plate to -150v through 1.8M.
3. When a Multi-Trace plug-in is in its ALT mode:
   a. The plate is connected to 225v through 10K in a 1A1.
   b. The cathode is tied to the base of a transistor (and DC ground through a blocking oscillator transformer primary) in a 1A1 and to ground in a CA.
4. The output waveform for a 1A1 is a positive going current pulse at pin 8 of the blue ribbon connector.
   a. A CA uses a negative going pulse at pin 16 of the blue ribbon connector.
5. With 10.4v fixed bias (from a divider), V764B is cut off.
6. The 15v step from the Sweep Hold-Off Multi (27v from the Sweep Switching circuit in DLY'D ALT) is differentiated in C760, L760.
   a. The positive going portion of the pulse is about 8v at V764B grid (about 6v in DLY'D ALT -- the Sweep Switching step has a T_R of about 1.5 μsec while the Hold-Off step rises in about 200 nsec).
   b. L760 provides a momentary high impedance grid load.
   c. Positive feedback through C768 provides some boost to the positive going pulse.

7. The positive going pulse drives V764B into conduction.
   a. The pulse of cathode current switches the 1A1.
   b. With a CA installed (operating in ALT mode) the plate pulls down about 60v (from 180v) to switch the plug-in.
8. The negative pulse on V764B plate disconnects D759 and coupled through C765, drives V764A grid.
   a. The negative charge on C765 discharges toward 225v to be limited at 22v by D759.
      (1) A faster recovery from the negative charge is achieved by the circuit in this manner.
9. The waveform on V764A plate is a 9v positive going pulse.
   a. D769 is decoupled.
   b. The pulse is coupled through C768 back to V764B grid as positive feedback.

D. Chopped Blanking Amplifier

1. V764A, the other half of the 6DJ8 used as a Sync Amp, serves as the Chopped Blanking Amplifier.
2. Quiescently the tube is conducting heavily -- 19.2 ma.
   a. 15.5 ma flows through R768, the load resistor.
   b. 3.7 ma flows through D769.
   c. The plate sets at 98v by virtue of D769.
      (1) V764A plate would pull down to 76v without D769.
3. When a Multi-Trace plug-in is switched to CHOP mode, the plate voltage and cathode return is removed from V764B.
   a. The tube offers no load to the Chopped Blanking circuit.

4. The waveform at pin 16 (in CHOP mode) differs greatly with plug-ins.

a. With a 1A1 plug-in it is a rather sad 1 mc square wave.

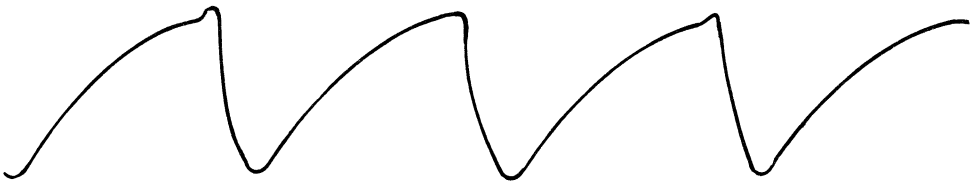
PIN 16

V764A GRID

V764A PLATE

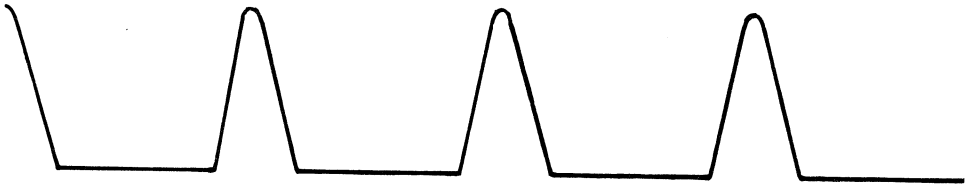
b. With a CA, the waveform approaches a positive going sawtooth of 100 kc.

PIN 16



V764A GRID

V764A PLATE

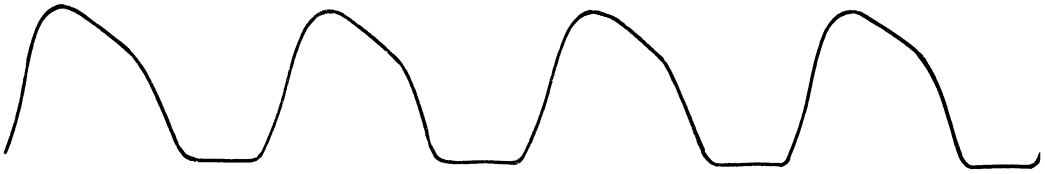


c. The M provides a rather clean positive going sawtooth.

PIN 16

V764A GRID

V764A PLATE



5. The negative excursion of these various waveforms disconnects D749, is differentiated somewhat in C765, R765, and drives V764A Grid.

6. As V764A current is reduced momentarily, D769 disconnects and the plate rises to 110v.

   a. This 12v pulse is the CHOP blanking waveform.

   b. The pulse is fed (AC coupled through .01 μf) to the CRT cathode.

   c. Since the 1A1 and M blanking pulses are rather broad, as much as 50% of the trace is lost in the CHOP mode.

7. A CHOPPED BLANKING switch (CRT circuit diagram) selects either CHOPPED BLANKING or Z AXIS modulation.

8. D769, which conducts except for the blanking pulse duration, presents the same load impedance to the CRT cathode in the CHOPPED BLANKING switch position as the closed link presents in the EXT CRT CATHODE position.

TYPE 547

XII. CRT AND HIGH VOLTAGE SUPPLY

A. The CRT and High Voltage circuit consists of the CRT, its regulated high voltage supply, the Unblanking Mixer and the controls necessary to focus and orient the display.

B. Outputs from the Regulated Supply

1. 8.15 kv for the CRT post accelerator anode.
2. -1.85 kv for the CRT cathode.
3. -1.9 kv (variable, floating supply) for the CRT grid.

C. Z Axis Modulation

1. AC coupled to the cathode.

D. Blanking and Unblanking

1. DC unblanking from A and B Sweep Generators.
2. Multi Trace Chop Blanking from a plug-in to the CRT cathode (AC coupled).

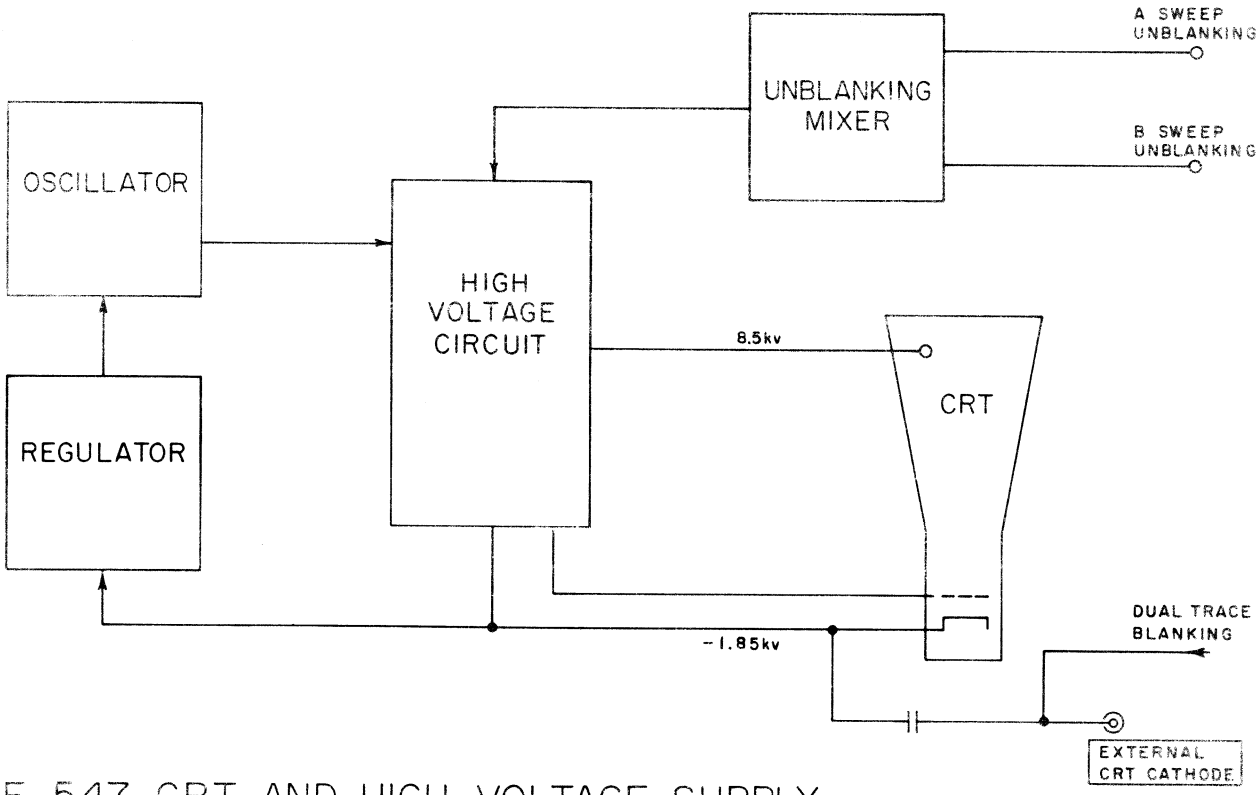
E. Controls, Front Panel

1. FOCUS
2. INTENSITY
3. ASTIGMATISM
4. TRACE ROTATION

F. Adjustments

1. HIGH VOLTAGE
2. GEOMETRY

G. Block Diagram



TYPE 547 CRT AND HIGH VOLTAGE SUPPLY BLOCK DIAGRAM

B-547-0050
4-28-'64 dl

H. Basic Circuits

1. Oscillator.
2. HV Regulator.
3. High Voltage Rectifiers.
4. CRT.
5. Unblanking Mixer.

I. Block Logic

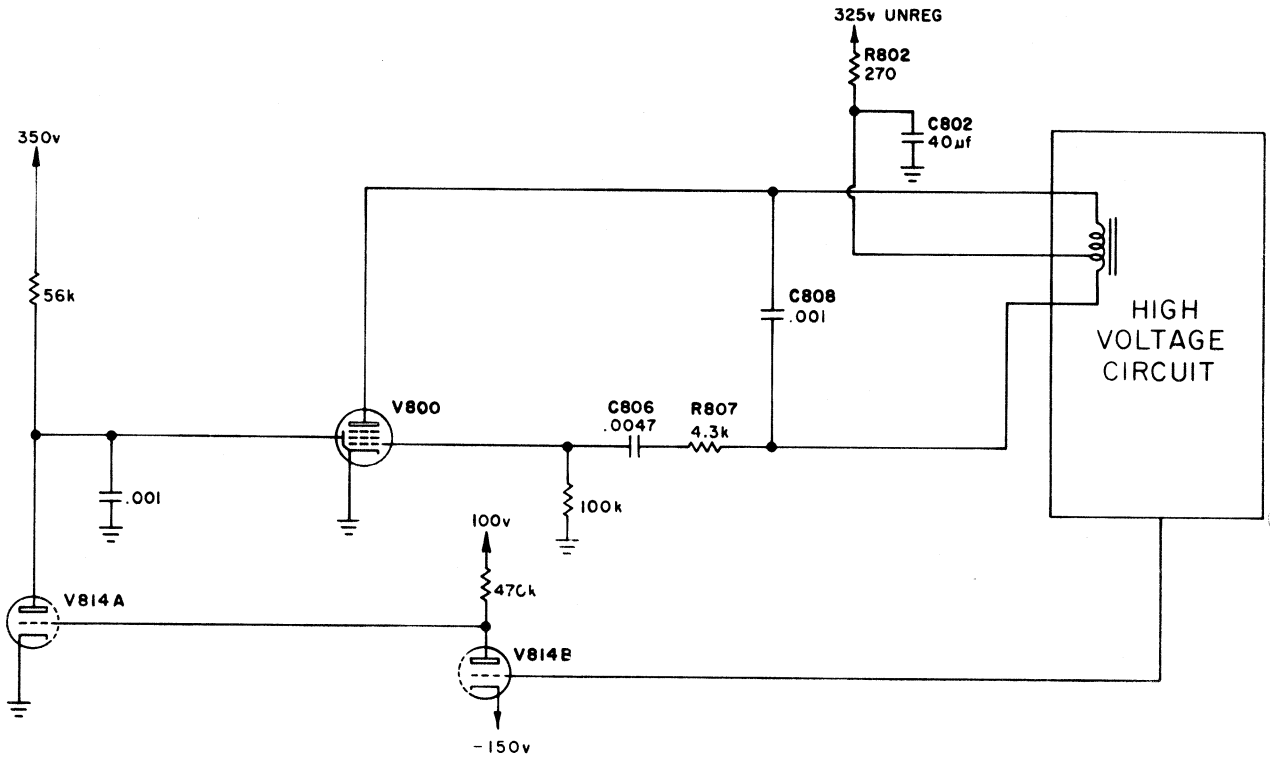
1. The free running oscillator develops a 50 kc sine wave.
2. The sine wave is stepped up in the high voltage transformer and rectified in three supplies.
3. 8.15 kv supplies the CRT post accelerator anode, -1.85 kv supplies the cathode and -1.95 kv feeds the grid.
4. A sample of the cathode supply is fed back to the regulator circuit.
5. The regulator controls the oscillator output.
6. A feedback loop is formed consisting of the oscillator, the cathode rectified supply, the regulator, and back to the oscillator.
7. The feedback loop keeps the HV supplies constant.
8. Unblanking information is superimposed on the CRT grid voltage to provide DC coupled unblanking during trace.

J. Oscillator

1. The oscillator is a 50 kc modified Hartley oscillator using a 6AU5 pentode.
2. C808 (with transformer stray C) and the HV transformer primary constitute the oscillator tank circuit.
    a. No attempt has been made to tune the oscillator to exactly 50 kc.
3. The waveform applied to the grid is a sine wave that reaches an excursion of -135v.
    a. As the tube draws grid current, it flattens the top of the waveform.
    b. The DC bias is -56v.

(1) Formed by the charge on C806 as the tube draws grid current.

4. Plate current is supplied from the 325v unregulated supply.



TYPE 547 CRT AND HIGH VOLTAGE SUPPLY OSCILLATOR

B-547-0051x
4-28-'64 dl

a. The typically 10v of ripple on the 325v supply is filtered to about 1v by R802, C802.

b. Although line voltage changes appear at the oscillator plate, there is little effect on the oscillator RF output.

(1) The high r_p of the pentode makes the current virtually independent of plate voltage fluctuations as a result of normal line voltage changes.

c. The line fluctuations and ripple that do modulate the output sine wave are removed in the regulator circuit.

5. The plate waveform is a fairly clean sine wave about 340v peak-to-peak.

a. The waveform flattens slightly on the bottom when the tube is driven into saturation.

6. Screen current is supplied from the 350v supply.

a. Correction voltage from the regulator amplifier controls oscillator current.

b. C803 prevents the regulator circuit from responding to the 50 kc oscillator frequency.

(1) Without C803, the regulator would stop the oscillator.

(2) C803 will allow the regulator to respond to changes in beam current from unblanking, Z axis modulation, etc., at frequencies below the 50 kc oscillator frequencies.

(3) Filtering in the high voltage divider and rectifier filtering will remove faster high voltage fluctuations.

c. C803 also provides a low impedance current source for 50 kc screen current requirements.

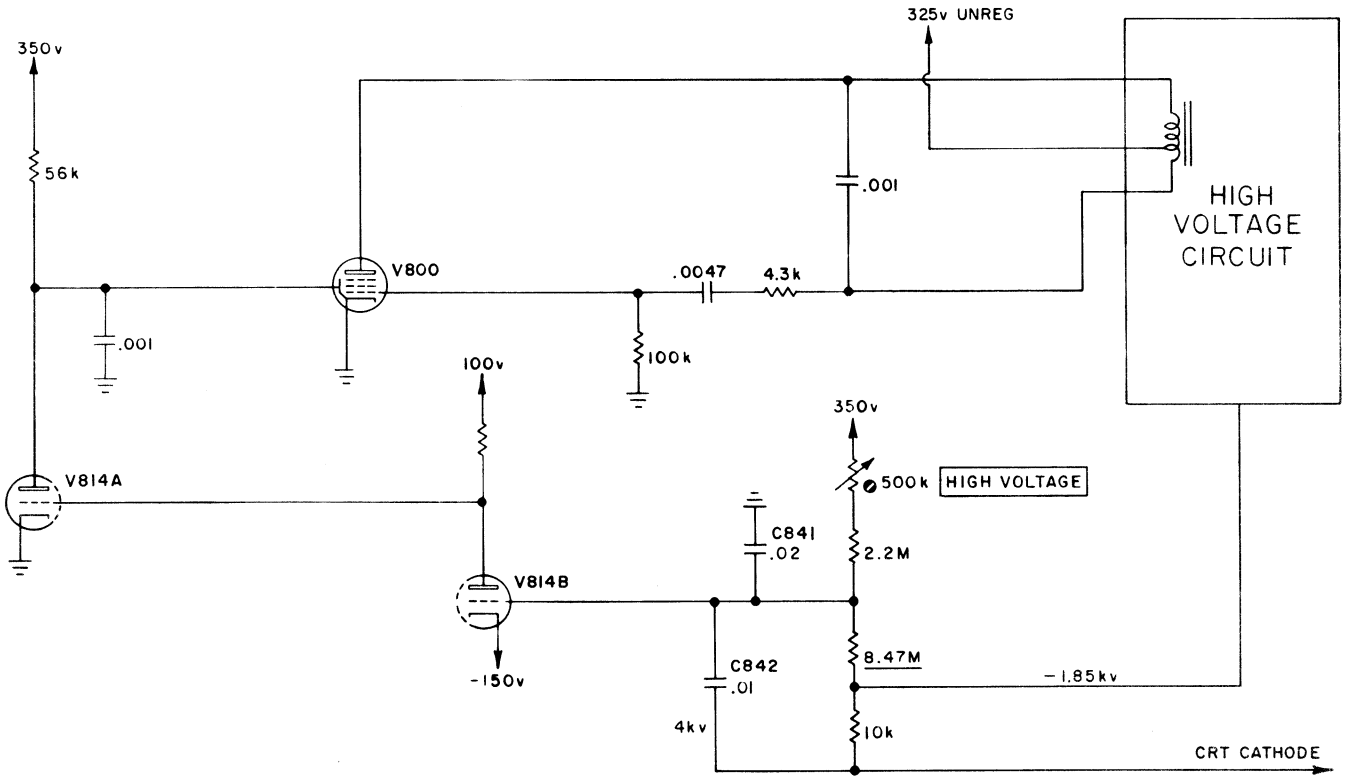
7. R807 limits grid current for tubes with various characteristics.

a. The resistance value is critical.

b. A deviation from the 4.3k value will cause the oscillator to block at about a 5 kc rate as C806 takes on too great a charge.

K. Regulator Amplifier

1. The Regulator Amplifier amplifies the errors voltage from the CRT cathode supply and applies it to the oscillator screen.



TYPE 547 CRT AND HIGH VOLTAGE SUPPLY REGULATOR CIRCUIT

B-547-0052 x
4-29-'64 dl

2. The amplifier is a two stage DC amplifier, using two halves of a 12AU7 dual triode.
   a. Gain of the amplifier is about 120.
3. The bias on V814B is about 10v (sets at -160v).
4. V814A grid sets at -2.5v.
5. High voltage adjustment:
   a. As resistance is decreased, V815B bias is decreased (grid moves up).
   b. The positive DC change is inverted and amplified in both V814A and V814B.
   c. The oscillator, V800, is biased to greater output.
   d. All the high voltage supplies increase.
   e. As the CRT cathode supply increases (toward -1900v), V814B grid returns to its original voltage.
      (1) As the system comprises an operational amplifier, the net result is increasing the output with virtually no change at the input grid (V814B).
6. The same feedback system operates to hold the CRT cathode voltage constant as beam current, component change, and line voltage changes attempt to change it.
   a. Since the CRT anode and grid transformer windings have a fixed relationship to the cathode supply, they also remain fixed.
   b. Component deterioration in the grid or anode supplies will not be compensated for by the regulator, however.

7. The divider between the CRT cathode and +350v is overcompensated by the AC divider composed of C842 and C841.

8. Line voltage changes introduced through the 350v supply are in proper phase to cancel changes in oscillator output as a result of oscillator tube heater voltage change.

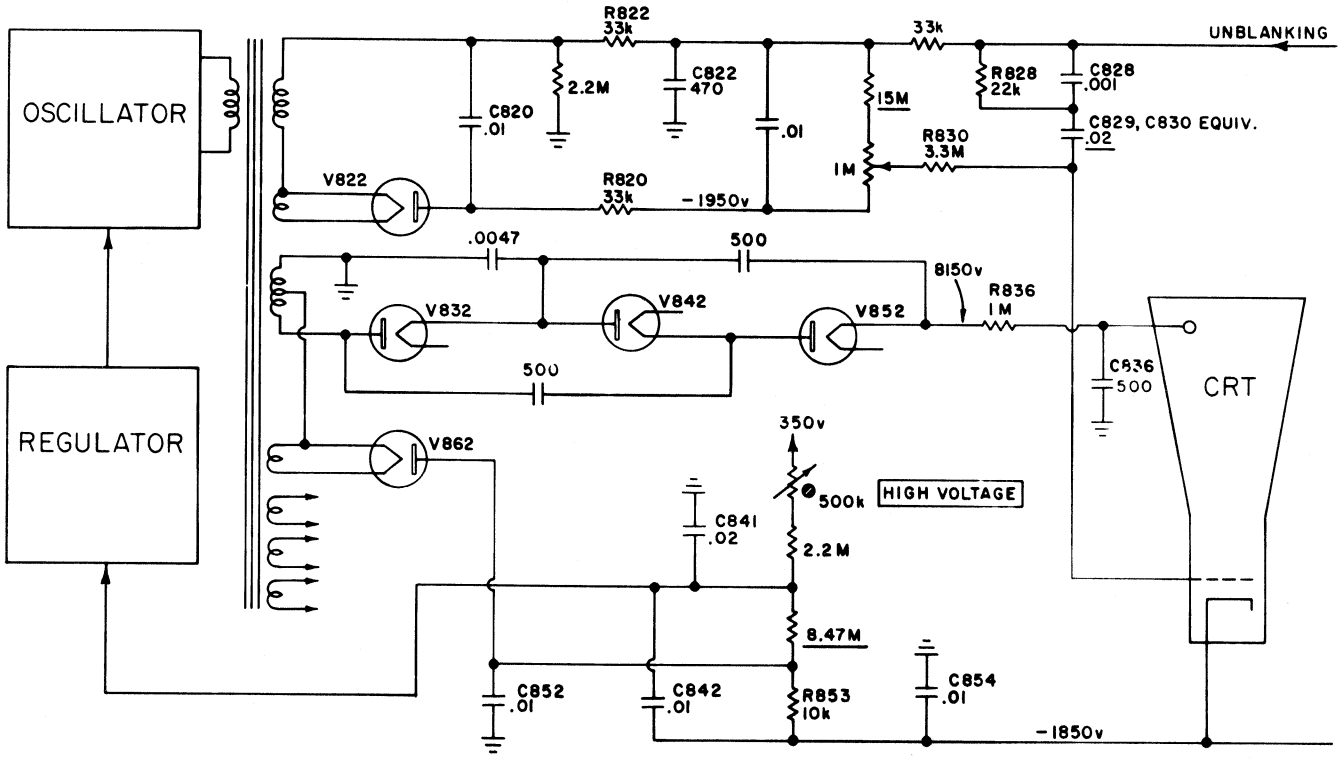
   a. The 350v supply may change as much as 350 mv with line voltage change.

9. Tying the divider to the 350v supply (instead of the 100v supply as in the 545A), provides a larger error signal off the divider.

   a. Loop gain is increased.

L. High Voltage Rectifier

1. The circuit consists of the high voltage transformer, five vacuum tube diodes and the filter circuits.



TYPE 547 CRT AND HIGH VOLTAGE SUPPLY
HIGH VOLTAGE CIRCUIT

B-547-0053 x
4-30-'64 dl

2. There are three high voltage supplies.
   a. 8.15 kv for the CRT post accelerator anode.
   b. -1.85 kv for the CRT cathode.
   c. -1.9 kv for the CRT grid.
3. The High Voltage transformer is TEK made.
   a. Since there are five filament windings, a flux unbalance is present (two windings on one side and three on the other).
   b. A flux equalizer composed of two reverse-wound windings on each side of the core equalizes the flux.
   c. The two high voltage secondaries are bifilar wound.
4. The Grid supply uses a single 5642 as a half wave rectifier.
   a. The entire supply is a floating supply to which 60v of unblanking is added, providing DC coupled unblanking to the CRT grid.
   b. The positive side of the supply receives the unblanking waveform (from -55v to +5v).
   c. The fast portions of the waveform bypass the supply to drive the CRT grid directly.
      (1) Stray capacitance from the HV transformer, wiring rectifier, etc., prevents the floating supply from following fast unblanking.
      (2) Total C is about .006 μf.
   d. A network of RC circuits couples the unblanking information across the floating supply and retains the shape of the waveform.

(1) C829, C830 are coupling caps for the unblanking voltage.

(2) R828 and C828 shape the front of the unblanking waveform (prevents a slight overshoot).

(3) R820 forms part of a DC divider to compensate for the .006 μf stray capacitance from the bifilar wound high voltage transformer.

e. R822 and C822 prevent 50 kc ripple from intensity modulating the CRT grid.

(1) Although the supply is filtered, the entire floating supply would move at 50 kc.

(2) The primary-secondary separation is 15 mils. The 50 kc in the primary is capacitively coupled to the grid supply secondary.

f. The INTENSITY control forms part of a 16M divider across the supply.

(1) The control picks off a portion of the -1950v for grid bias.

(2) Range is from -1950v to -1828v (approximately).

(3) CRT cut-off bias ranges from -85v to -95v.

(4) The control offers a bias range (grid voltage relative to cathode voltage) of -100v to +22v.

(5) CRT cathode degeneration and grid current limiting by R830 would prevent CRT damage.

(6) The wide range of bias allows for variations in supply voltages and rectifier tube aging.

g. R830 isolates the floating supply from the AC coupled fast portions of the unblanking waveform.

5. The CRT post accelerating anode supply uses three 5642's as a half wave voltage tripler*.

a. +8150v is supplied at about 350 μa maximum.

b. R836, C836 filters the 50 kc ripple.

(1) It prevents 50 kc radiation off the face plate.

6. The CRT cathode supply uses a single 5642 as a half wave rectifier to deliver -1850v at 2.5 ma maximum.

a. A tap off the anode winding of the HV transformer is used.

b. The 50 kc supply is filtered by C852, C854 and R853.

c. A series of resistors totaling 11.12M bleed the cathode supply to ground.

d. The bleeder also serves as a divider from which error voltage to the Regulator is taken.

(1) The DC level is divided down to -160v where it drives V814B grid.

(2) C842 and C841 compensate the divider and together help bypass fast transients to ground.

e. The cathode supply is adjusted by the HIGH VOLTAGE adjust.

M. CRT Circuit

1. The CRT is a T5470* aluminized five inch flat-faced CRT with electrostatic focus and deflection. It has a 200 megohm helix that provides post-deflection acceleration with a minimum of compression. It features a lighted internal graticule.

* Typical Oscilloscope Circuitry, page 12-8.

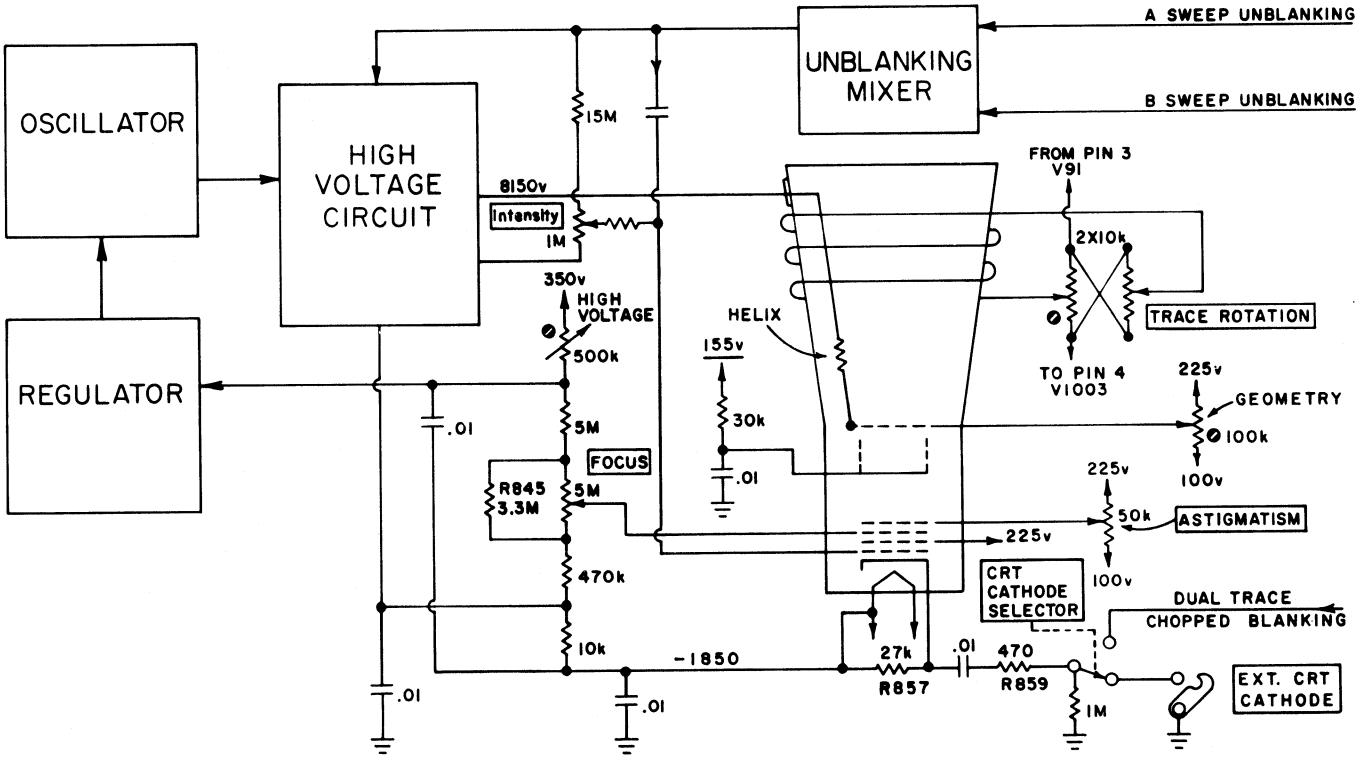
* See CRT IRB and story in appendix.

a. A P31 phosphor is normally supplied with the production type 547.

b. Display area is 6 x 10 cm.

2. Total accelerating potential is 10 kv (CRT rating is 13,200v maximum).

3. Spot size is nominally 9 mils over the entire display area.



TYPE 547 CRT AND HIGH VOLTAGE SUPPLY
CRT CIRCUIT

B-547-0054 x
5-1-'64 dl

4. INTENSITY is controlled by a 1M pot as part of the 16M bleeder across the CRT grid supply.
   a. A range of -1950v to -1828v is supplied.
   b. Relative to the cathode, the range is -100v to +22v.
   c. CRT cut-off bias varies from -85v to -95v.
5. The 60v unblanking waveform biases the tube on during trace.
6. The FOCUS control is part of the CRT cathode supply bleeder.
   a. The control is a 5M pot shunted by a 3.3M resistor.
      (1) Without the FOCUS pot, the bleeder has a 5% tolerance.
      (2) A dependable, better than 20% tolerance, 5 meg pot is not readily available.
      (3) A closer than 20% tolerance bleeder string is desirable, however, as it provides a greater useful range of the FOCUS control.
      (4) R845, a 5% component, provides an 8% tolerance bleeder string, allowing the FOCUS control range to be used for controlling focus rather than compensating for bleeder resistor drift.
   b. Range is from -1350v to -1720v (130v to 500v relative to the cathode).
7. An insulated cap over the FOCUS and INTENSITY control pots protect from shock hazard.
8. The ASTIGMATISM control is a 50k pot with a range of 100v to 225v (1950v to 2075v relative to the cathode).

9. The GEOMETRY adjust is a 100k pot with a range of 100v to 225v.
   a. Varies the potential on the lower helix.
10. TRACE ROTATION control is a dual 10Ω pot cross connected and placed in series with V91 and V1003 heaters.
   a. This is part of the DC heater string connected to the 100v regulated supply.
   b. The coil is composed of 400 turns of No. 23 wire wrapped around the center of the CRT under the mu-metal shield.
   c. DC resistance is about 11Ω.
   d. 150 ma through the circuit provides up to ±47 ma through the coil.
11. A helix winding with a minimum resistance of 200M is connected internally between the post accelerator anode and the lower helix pin.
12. The vertical deflection plate shield is connected to an equivalent 30k to 155v (2005v with respect to the cathode).
13. The cathode has its own -1850v supply.
   a. The CRT heater is elevated to -1850v to reduce the chance of cathode heater short.
14. Z axis modulation is available through a rear panel EXTERNAL CRT CATHODE jack.
   a. The input is designed for use with marker pulses.
   b. 5v will usually be adequate to modulate the display.
      (1) A 20v square wave (the cal signal for example) will pull the HV supply out of regulation.

c. A link grounds the jack when not in use.

(1) With the link removed, the beginning of the trace will be dimmed at fast sweep speeds.

(2) Capacitive coupling, grid to cathode, will lift the cathode at the start of unblanking. The C must discharge through R857 to return to normal intensity.

d. A CRT CATHODE SELECTOR switch on the rear panel selects either DUAL TRACE CHOP BLANKING from a multi trace plug-in or input from the EXT CRT CATHODE jack.

e. R857 isolates the Z axis drive (and chop blanking) from the high voltage supply.

f. Impedance looking into the EXT CRT CATHODE jack is about 26k at low intensity, dropping to about 23k at high intensity.

(1) R859 in series with the parallel combination of R857 and the CRT cathode transimpedance.

g. Z axis input is AC coupled (.01 μf).

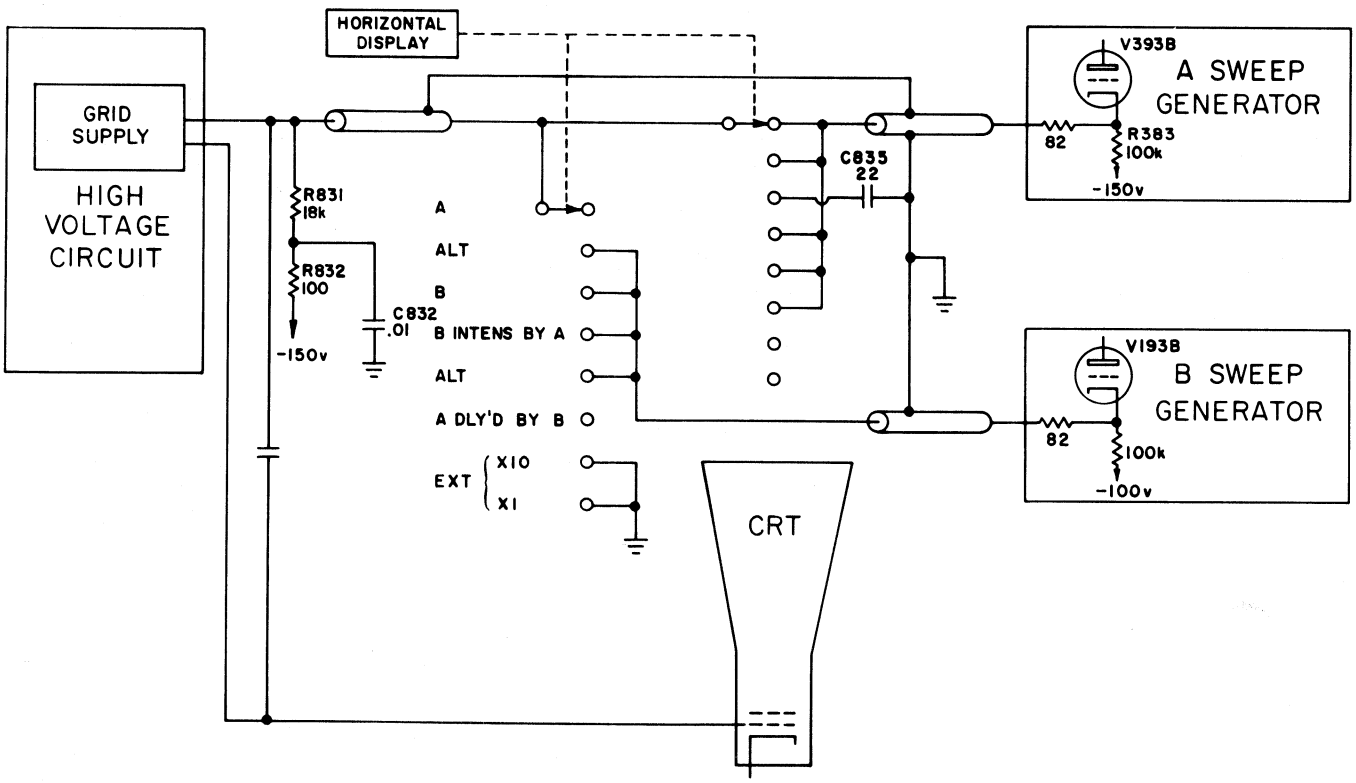
h. R859 damps ringing at the start of trace.

(1) The grid-to-cathode capacitance together with lead inductance would ring as the unblanking pulse tried to pull on the CRT cathode.

15. The dual trace chop blanking pulse is about 20v peak-to-peak.

N. Unblanking Mixer

1. The Unblanking Mixer combines A Sweep and B Sweep unblanking to satisfy unblanking requirement in the various modes of the HORIZONTAL DISPLAY switch.



TYPE 547 CRT AND HIGH VOLTAGE SUPPLY UNBLANKING MIXER

B-547-0055x
5-4-'64 dl

2. The unblanking waveform is a 60v peak-to-peak pulse (-55v to 5v) with a risetime of about 27 nsec.

3. When not in use, the unblanking CF's in the Sweep Generator circuits are long-tailed through 100k resistors to -150v.

   a. This provides 1 to 1-1/2 ma "standby" current.

4. When the CF is connected (by the HORIZONTAL DISPLAY switch) to the CRT gird, R831 becomes the CF cathode resistor.
   a. If both CF's are connected in parallel, they share the 18k cathode resistor.
   b. Current, therefore, is virtually the same whether one or two CF's drive the unblanking circuit.
   c. R832, C832 is a decouple network that keeps unblanking information out of the -150v power supply.
5. HORIZONTAL DISPLAY mode connections.
   a. In A mode only, the A Sweep Unblanking CF is connected.
      (1) The cathode resistor is R831 in parallel with the 100k (R383, A Sweep Generator).
   b. In A-ALT-B mode, both A and B Sweep Unblanking CF's are connected.
      (1) The CF's are literally in parallel.
      (2) The two CF's have an equivalent 13.2k to -150v.
      (3) Only one CF conducts at a time, however.
   c. B mode connects the B Sweep Unblanking CF to the CRT grid circuit.
      (1) C835 is connected from the unblanking bus to ground.
      (2) The cap compensates for the absence of capacitance from the A Sweep CF and lead capacitance in this mode.
      (3) This is the only sweep mode where the A Sweep CF is not connected.

d. B INTENS BY A mode has both CF's connected in parallel.

(1) The B Sweep unblanking pulse has a -17v to +4v positive excursion depending on the BRIGHTNESS control setting*.

(2) When A Sweep unblanking pulse lifts the common cathodes to +5v, the A Sweep portion of the display appears as an intensified zone.

(3) A and B unblanking waveforms do not add algebraically, but follow the more positive grid of the parallel CF's.

e. In the B INTENS BY A-ALT-A DLY'D BY B mode, both CF's are connected.

(1) The Unblanking Gate in the B Sweep Generator keeps the B unblanking circuit turned off during A DLY'D BY B display.

f. In the A DLY'D BY B mode, only the A Sweep CF is connected.

g. In the EXT modes, the top of the grid floating supply is grounded, unblanking the CRT.

(1) Intensity is slightly less than A Sweep unblanking and slightly more than B unblanking (nominal setting of the BRIGHTNESS control).

* See B Sweep Unblanking Amplifier.

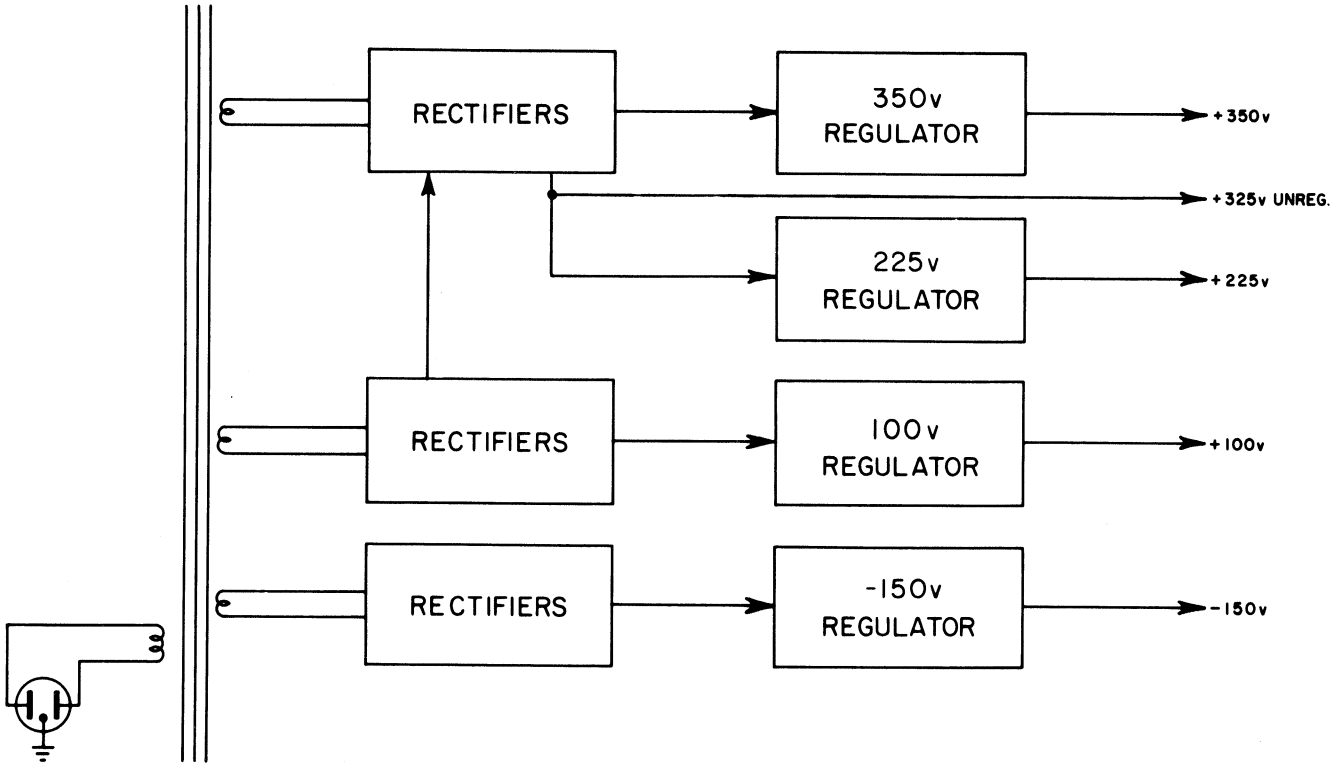
TYPE 547

XIII. LOW VOLTAGE POWER SUPPLY

A. The low voltage power supply provides four regulated voltage sources for use in scope main frame and plug-ins and a 325v unregulated source for use in the CRT circuit.

1. All supplies will regulate with the plug-in removed.
2. The supplies will regulate with primary voltages from 115 ± 10% (103.5-126.5) (115v connection).

B. Block Diagram



TYPE 547 POWER SUPPLY
BLOCK DIAGRAM

B-547-0070
4-27-'64 ms

C. Block Logic

1. A common power transformer supplies all regulated supplies and heater needs in the scope main frame and its plug-in.

2. Regulated supplies:

   a. -150v, ±2%, 3 mv ripple.

   b. +100v, ±2%, 7 mv ripple.

   c. +225v, ±2%, 3 mv ripple.

   d. +350v, ±2%, 20 mv ripple.

3. Unregulated voltage source.

   a. 325v.

4. The -150v supply uses an OG3 glow tube as reference.

5. The 100v, 225v and 350v supplies use the regulated -150v as reference.

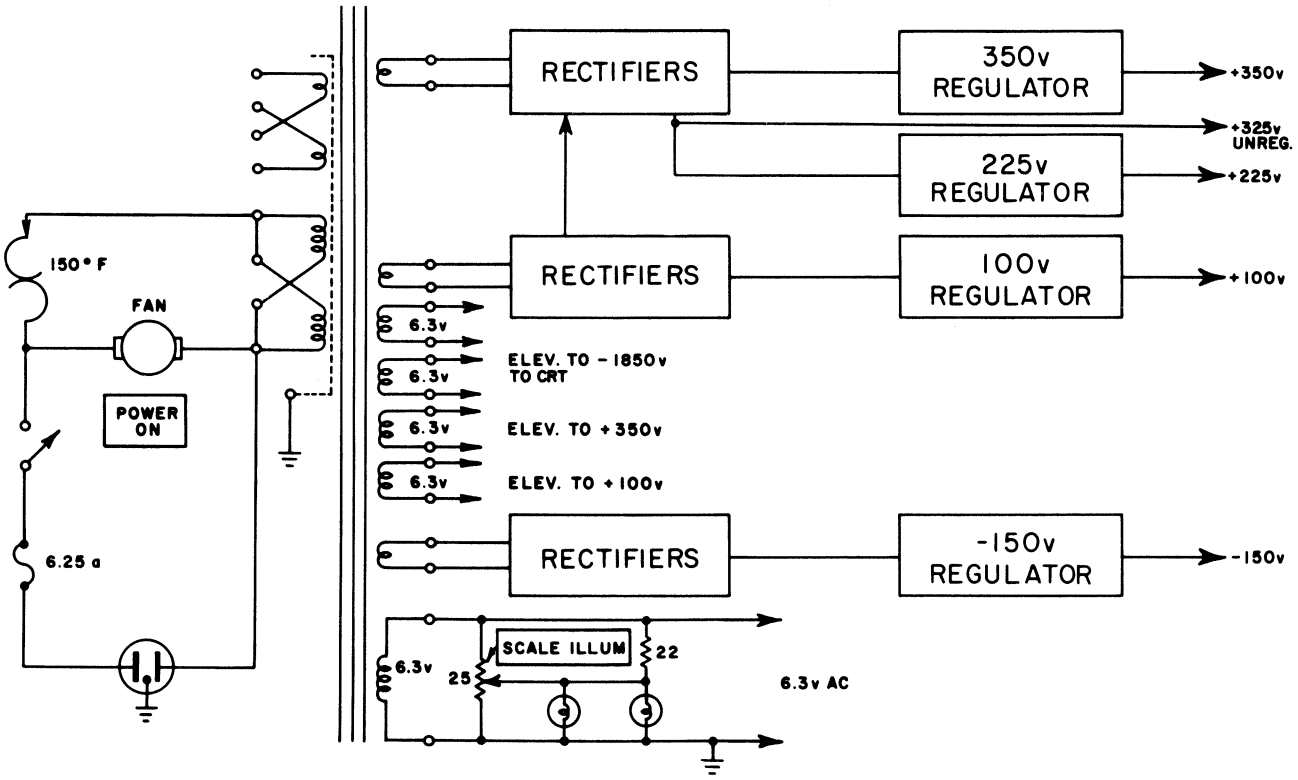
6. The 325v source is the unregulated output from the 225v rectifier.

7. Three sets of bridge rectifiers* provide DC for the four regulated supplies.

8. The 225v rectifiers stack on the 100v rectifiers and the 350v rectifiers stack on the 225v supply.

* Typical Oscilloscope Circuitry, page 12-5.

D. Transformer Circuit



TYPE 547 POWER SUPPLY
TRANSFORMER CIRCUIT

B-547-0071
4-27-64 ms

1. The power transformer is Tek made.
   a. The primary is insulated to 600v.
2. Besides the three windings for the bridge rectifiers, five heater windings are provided.
   a. 6.3v, .6a for CRT heater.
      (1) Elevated to -1850v.

b. 6.3v, 3.25a for 225 and 350v regulator tubes.

(1) Elevated to 350v through 150k.

c. 6.3v, 1.5a for the Horizontal Amp output tubes.

(1) Elevated to 100v through 100k.

d. 6.3v, 7.6a for the B Sweep and power supply chassis and the Power On light.

e. 6.3v, 8.8a for the A Sweep chassis, the F and I deck, the Vertical driver tube and the graticule lights.

(1) The winding also goes to pins 13 and 14 of the blue ribbon connector for plug-in AC heaters.

(2) The LINE TRIGGER voltage is fed from this winding.

3. A detachable 3 wire power cord is supplied.

4. One side of the power line is interrupted by the Power On switch, a fuse and the thermal cutout.

a. The fuse is a 6.25a, 3AG "Slo-Blo".

b. The thermal cutout will open at 150°F.

(1) When the transformer primary is connected from 115v, the fan will continue to run after the cutoff opens.

(2) When connected for 230v, the fan will turn off with the cutout.

(3) The cutout resets automatically when temperatures return to normal.

5. A 35W, 1500 RPM fan provides forced air ventilation.

a. The fan is connected across the 115v line ahead of the thermal cutout.

b. When the transformer primary is connected for 230v, the fan is connected to a 115v tap on the primary winding.

c. The fan operates from 50 to 60 cps.

6. The transformer has two main primary windings.

a. When connected in parallel, the scope will operate on 115v.

b. When connected in series, the scope will operate on 230v.

c. Two extra windings allow additional voltages of 108v, 122v, 216v, 244v.

7. Line frequency is 50 to 60 cps.

a. Line frequency can be increased to 400 cps with an AC to AC converter mod to drive the fan (50-60 or 400 cps -- not continuous).

8. Regulation specs are optimized at 1% sine wave distortion.

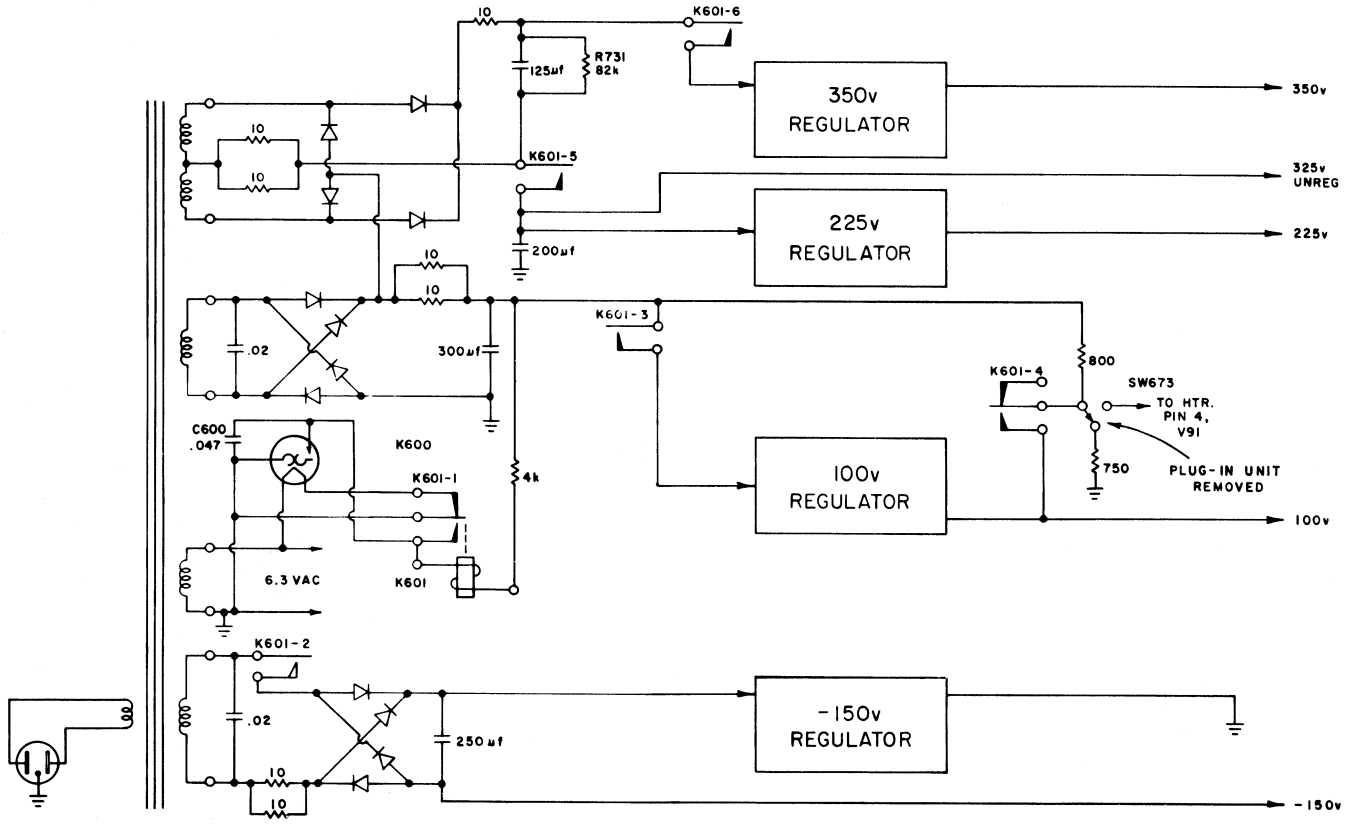
a. Typical acceptable distortion is 2% to 2-1/2%.

b. Increased distortion will narrow the range of line voltages over which the scope will regulate.

c. Saturable reactor regulators (for example) may distort the sine wave sufficiently to prevent the Low Voltage Power Supply from meeting regulation specs.

E. Time Delay Relay

1. All DC supplies remain open for approximately 30 sec to allow the heaters time to warm up.



TYPE 547 POWER SUPPLY
DELAY RELAY

B-547-0072-x
5-6-'64 dl

2. K600 is a 30 sec thermal relay and K601 is a 22-1/2 ma (rated 15 ma to 30 ma) DC relay.

   a. K601 has a 3600Ω coil and in operation has 81v across it.

3. When the instrument is turned on, 6.3v AC is connected through K601-1 to K600 heaters.

a. The thermal relay heater takes about 30 seconds to close.

b. K601 coil is returned to ground through the thermal relay.

c. As K601 coil is tied to the unregulated 100v supply rectifiers, through 4k, 30 ma flows through the coil closing the relay.

d. K601-1 opens K600 heater return allowing the thermal relay to cool.

e. K601-1 now becomes a holding relay supplying holding current through its own contacts.

(1) The contacts actually make before breaking assuring its holding ability.

(2) A momentary interruption of power will open the holding contacts.

(3) The thermal relay then must turn K601 on again after a 30 sec delay.

4. During the 30 sec warm-up period, all regulated supplies are open.

a. K601-2 opens the -150v rectifier circuit.

b. K601-3 disconnects the 100v regulator.

(1) The rectifiers are still connected.

(2) The 100v supply energizes K601.

(3) The 100v supply feeds the DC plug-in heaters.

c. K601-4 bypasses the 100v regulator and preheats the plug-in heaters.

d. K601-5 disconnects the 225v regulator.

e. K601-6 disconnects the 350v regulator.

(1) The 225v/350v rectifiers are still connected.

(2) R731 bleeds the supply.

5. The relay is connected so the 100v and 350v filter capacitors charge when the scope turns on and the -150v and the 225v capacitors charge when the relay closes.

a. Delaying part of this current surge prevents a single current surge that could blow the primary fuse or damage the power switch.

6. C600 reduces contact arcing and protects the relay contacts (both K600 and K601-1).

F. +100v Supply

1. The +100v supply is a series regulated supply* fed by a full wave silicon bridge rectifier.

2. The supply delivers an average of 350 ma to 400 ma (depending on the plug-in).

a. A connection to pin 10 of the blue ribbon connector (through 100Ω decoupling) supplies the plug-in; as an example, 55 ma for a Type 1A1.

b. About 150 ma is provided for the DC heater string.

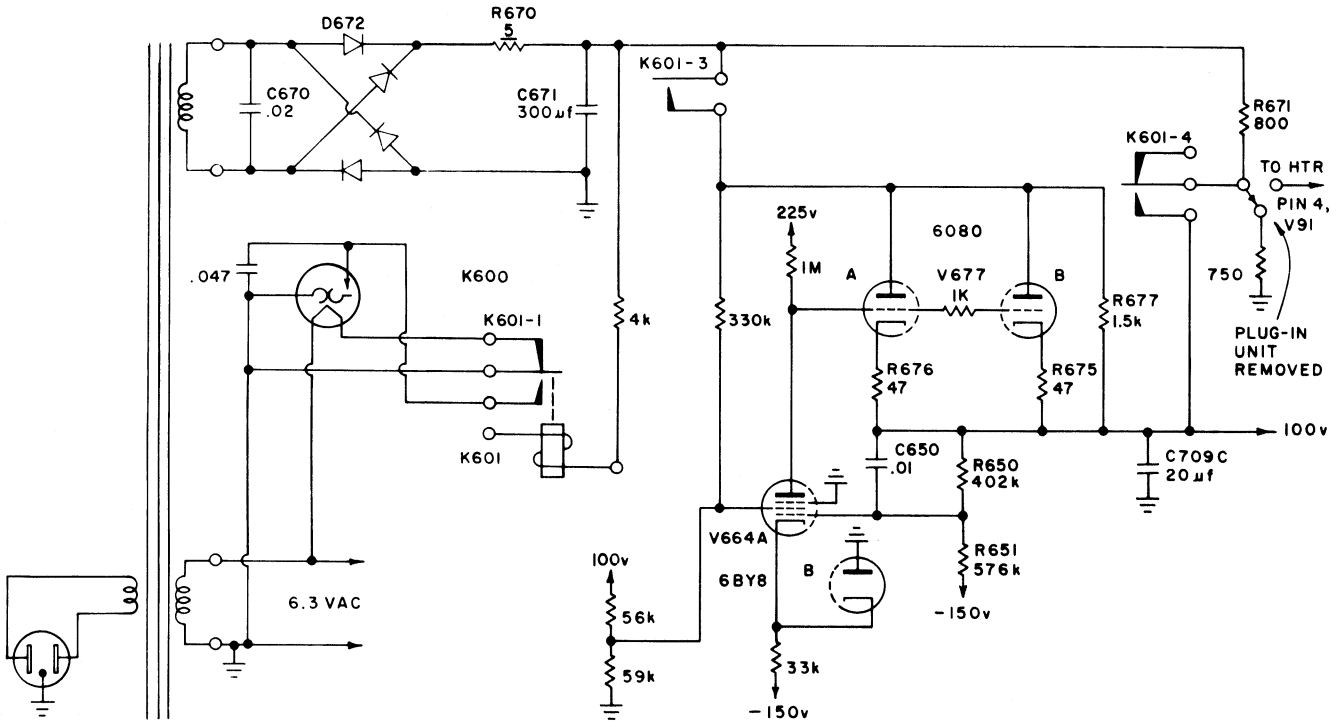
(1) The string includes V91 (B Sweep Miller tube), V1003 (Vertical Amp input CF's) and the trace rotation coil.

* Typical Oscilloscope Circuitry, page 7-3.

(2) The portion of the series string in the main frame drops the 100v to 75v.

(3) The 75v at 150 ma is tied to pin 15 of the blue ribbon connector to supply the plug-in DC heaters.

c. The main frame requires about 145 ma.



TYPE 547 POWER SUPPLY
+100v SUPPLY

B-547-0073x
5-7-'64 dl

3. During the warm-up (the 30 sec before the time delay relay closes) the DC string bypasses the regulator and dropped by R671 ties directly to the rectifier.
   a. R671 provides a voltage drop normally supplied by the regulator circuit.
4. A spring return switch places a 750Ω dummy load on the supply when the plug-in is removed.
   a. The switch mounted at the rear of the plug-in housing is activated when the plug-in is inserted.
   b. The supplies stay in regulation.
   c. The switch may be activated by hand (by pulling forward to the holding position) if, during calibration, a plug-in extension is used.
5. The supply uses a 161v RMS transformer secondary rated at .9a.
6. A full wave silicon bridge supplies 205v DC (at 115v line).
   a. The rectifier diodes are 152-047 RCA 1N2862 silicon 500 ma diodes with a PIV rating of 400v.
   b. C670 reduces silicon switching transients.
   c. C671 filters the rectifier output.
7. R670A and R670B provide an equivalent 5Ω, 4W (two 10Ω in parallel) in series with the bridge rectifier.
   a. The resistance provides surge protection as C671 charges during initial turn-on.
      (1) A turn on coincident with a voltage peak can draw as much as 30a through the 5Ω resistor.

b. The two 10Ω resistors at 2 watts provide a fuse should C671 short.

c. The 5Ω provides a convenient voltage drop for checking current of the supply.

(1) There is about 2v drop with a 1A1 plug-in in use.

8. Both halves of a 6080 dual triode placed in parallel function as the series regulator tube.

9. V664A, the pentode section of a 6BY8 is the error amplifier.

10. V664B, the diode section of the 6BY8, compensates for the grid cathode bias of V864A during line voltage changes.

a. A test instrument had a cathode change of 150 mv for a line voltage change of 105v to 125v while the grid had no perceptable change.

11. A voltage divider composed of R650 and R651 is bridged between the 100v regulated output and the regulated -150v.

a. -150v serves as reference voltage.

b. V664A grid is tied to the junction of the two resistors at -2.4v.

c. Any change in voltage at the 100v bus, whether from load change, line voltage change or ripple, will appear as an error voltage at V664A grid.

12. Assume an increased load current requirement starts to drop the 100v output.

a. The error voltage increases the negative bias of V664A.

b. As the pentode current decreases the plate raises gain times as far as the error voltage on the grid.

c. As the pentode plate rises it biases V677 to greater conduction.

d. The load current requirement is satisfied and the 100v bias returns to the proper potential.

e. V664A grid returns to its original level.

f. There is virtually no change in the grid voltage.

(1) $\Delta e_g = \frac{\Delta E_o}{\text{Loop Gain}}$

Where Δe_g is the grid voltage change, ΔE_o is the regulated output voltage, and the loop gain is about 200.

13. The regulator can be considered an operational amplifier that serves to maintain the ohms law voltage division across voltage divider (R650, R651).

a. Since the bottom of the divider is referenced to -150v and V664A grid sets solidly at -2.4v, the accuracy of the voltage at the 100v output is a direct function of divider resistor accuracy.

b. All sensing divider resistors are 1% precision resistors.

c. If, as an example, R650 was 1% high and R651 was 1% low, the feedback circuit would maintain accurage voltage division across the divider and the 100v bus would raise to 102.2v.

14. V664 has a gain of about 200.

    a. The plate sets at about 75v with the line at 115v.

        (1) This potential will change with line voltage from 87v at 105v line to 57v at 125v line.

    b. The cathode sets at 0.8v.

    c. Only about 145 μa of plate current flows.

    d. About 5v of ripple appears in the plate.

    e. Screen voltage is 50v (115v line).

15. Ripple content of the regulated output can be reduced by introducing ripple from the unregulated bus to the pentode screen.

    a. A 300k introduces about 400 mv of ripple at the screen.

        (1) This includes about 50mv of degeneration from grid action that is canceled by the screen injected ripple.

    b. Without R667 about 12 mv of ripple would be present on the 100v regulated bias.

    c. Where in normal operation the regulator must sense an error in the output before correction can occur, the screen injected ripple "anticipates" the need and removes the ripple before it appears in the output.

16. C650 couples transients across R650 -- a speed-up cap -- it overcompensates the divider.

    a. A leaky capacitor would effectively reduce the value of R650.

    b. The sensing divider ratio would be changed and output voltage would be reduced.

17. R677 and R671 carry the static load current.

    a. Total static current through R677 and R671 is about 195 ma at 115v line.

18. R675 and R676 equalize the current balance in V677A and V677B.

    a. They are 47 ohm 5% resistors.

    b. They allow for differing bias requirements.

19. C709C is located on the Sweep Deck.

    a. It bypasses sweep transients that are isolated from the regulated supply by lead inductance.

20. When either sweep is running a 4 mv positive going notch appears on the 100v regulated bus during hold-off.

    a. Switching transients at the start and end of the notch may reach 25 mv peak-to-peak.

21. The calibrator will introduce a 3 to 5 mv square wave to the 100v regulated output with switching transients to 15 mv.

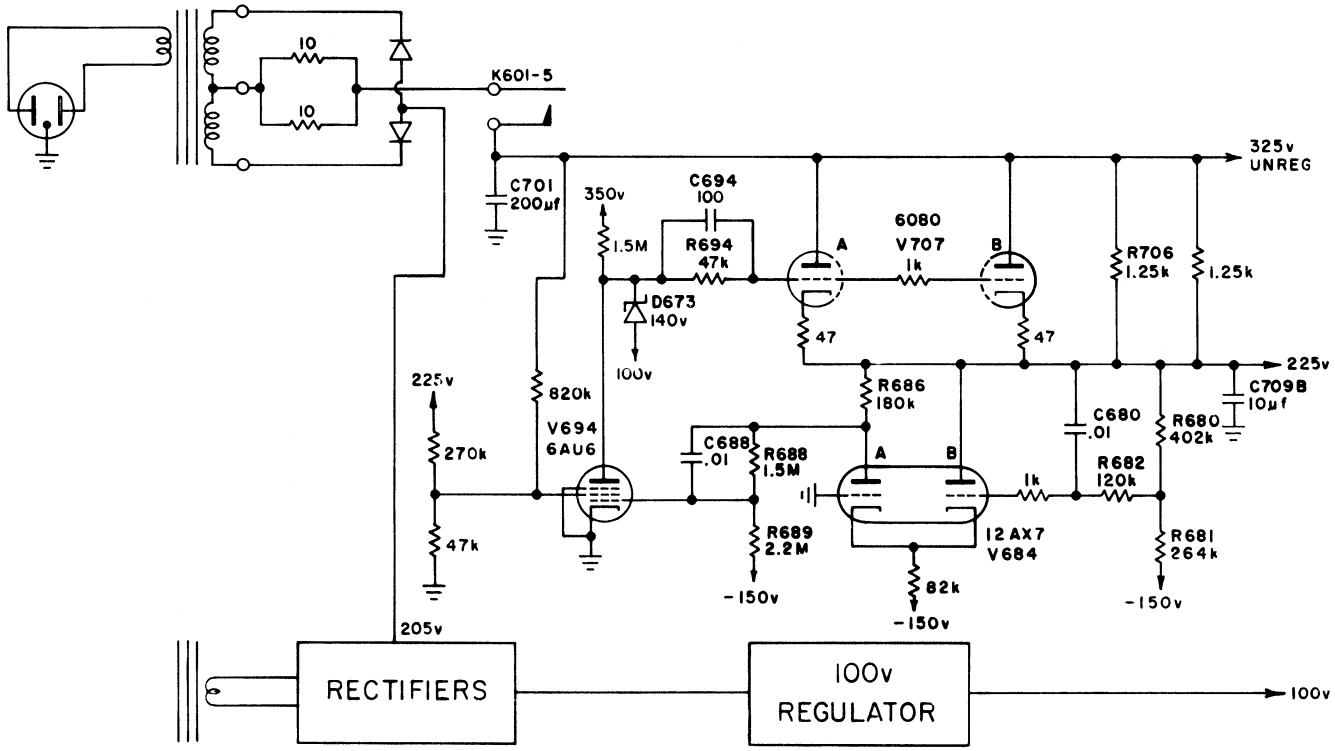
22. Dynamic impedance of the regulated output is about .3Ω.

    a. Measured at the top of the sensing resistors.

    b. $Z = \frac{\Delta e}{\Delta i}$.

G. +225v Supply

1. The 225v supply is a series regulated supply fed by a full wave silicon rectifier.



TYPE 547 POWER SUPPLY
+225v SUPPLY

B-547-0074 x
5-11-'64 dl

2. The 225v output has 3 mv ripple spec so additional gain is required in the regulator error amplifier.

   a. In addition to a 6AU6 pentode amplifier, a cathode coupled triode amplifier contributes a gain of about 15.

3. The supply provides about 340 ma.

4. The output is fed (via 100Ω decoupling) to pin 11 of the blue ribbon connector.
   a. About 37 ma is used in a 1A1.
5. The supply shares a transformer secondary winding with the 350v supply.
   a. The center tapped secondary winding has 113v each side.
   b. Rated at .42 a.
6. Two silicon diodes connected as a conventional full wave rectifier supply the 225v regulator with about 355v DC (at 115 line).
   a. The diodes are RCA 1N3194 750 ma silicon diodes with a PIV of 400v.
   b. The diodes also form part of the 350v supply bridge rectifier.
   c. The 225 supply rectifier is stacked on the 100v rectifier.
      (1) The minus side of the rectifier sets at about 205v (115v line).
      (2) This point will vary from 180v at 105v line to 225v at 125v line.
   d. C701 filters the rectifier output.
7. Regulator operation is basically the same as the 100v regulator.
8. The cathode coupled amplifier (V684, a 12AX7 dual triode) is used as a comparator.
   a. It compares error voltage from the sensing resistors (R680, R681) on one grid with ground on the other grid.

b. The error voltage is taken across R686 (the plate load resistor) amplified by a factor of 15.

(1) The cathode coupled amplifier does not invert the error voltage.

c. C680 provides a path for fast voltage changes from the 225 regulated bus to V684 grid.

(1) R682 provides a high impedance grid load for C680 to drive.

(2) R680, R681 form a grid load impedance of 160k.

(3) R682 increases the impedance to 280k.

d. V684A plate sets at approsimately 105v.

e. The long-tail cathode draws about 1.8 ma.

(1) The cathode sets at .5v.

(2) The grid sets at -1v.

9. A voltage divider (R688, R689) divides down from the 105v found on V684A plate to the -1.3v bias required for V694.

a. The error signal is also attenuated by the divider.

b. C688 bypasses the divider for fast changes.

10. The pentode error amplifier is a 6AU6.

a. It has a gain of about 200.

(1) 1.5M plate load resistor contributes to high gain.

b. The plate sets at about 180v (115v line).

(1) About 6v peak-to-peak ripple is present.

c. Ripple is injected at the screen to cancel output ripple.

11. Series regulator configuration using a 6080 is the same as the 100v regulator circuit.

12. D673 is a 140v zener that is used as a limiting diode.

    a. V707 grids cannot raise above 240v if V694 is removed from the socket.

    b. A conventional diode could have been used if a 240v supply had been available.

    c. Limiting prevents the 225v bus from rising high enough to blow the transistors in the cascode Vertical Output amplifier.

    d. R694 limits zener current (preventing D673 burn out) if V707 has momentary internal element flashover.

    e. C694 conducts fast changes to V707 grid.

13. Shunt resistor R706 carries about 200 ma during average load and average line voltage conditions.

14. C709B is located on the Sweep chassis.

    a. It bypasses sweep switching transients isolated from the regulated supply by lead inductance.

15. Dynamic output impedance is about .01Ω.

H. +325v Unregulated

1. The 325v unregulated supply is the filtered but unregulated output from the 225v rectifier.

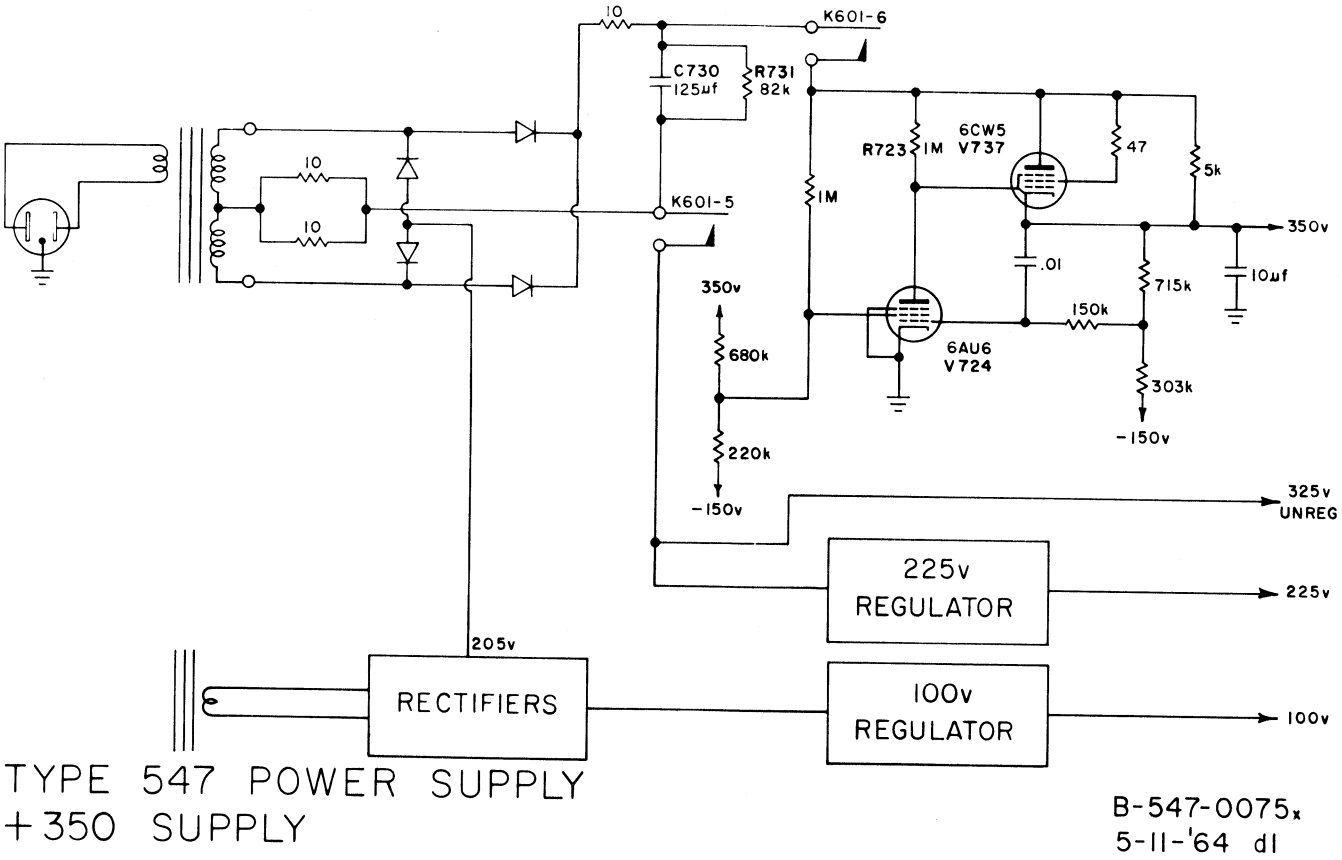
2. Although it is called 325v, the bus will vary from 320v at 106v line to 395v at 125v line.

3. About 9v of ripple is present.

4. The unregulated voltage is used only in the oscillator in the CRT high voltage supply.

I. +350v Supply

1. The 350v supply is a series regulated supply fed by a full wave silicon bridge rectifier.



2. The 350v output has a 20 mv ripple spec.

3. The supply provides about 60 ma.

   a. The output ties to pin 12 of the blue ribbon connector (through 100Ω decoupling).

   b. Some plug-ins, including the 1A1 do not use the 350v supply.

4. The supply shares the tapped transformer winding with the 225v supply.

5. There are two ways to consider the rectifier configuration.
   a. It is a full wave bridge rectifier stacked on the 100v unregulated supply and tapped in the middle to supply the 225v regulator.
   b. It can also be considered a two diode full wave rectifier stacked on top of the 225v supply.

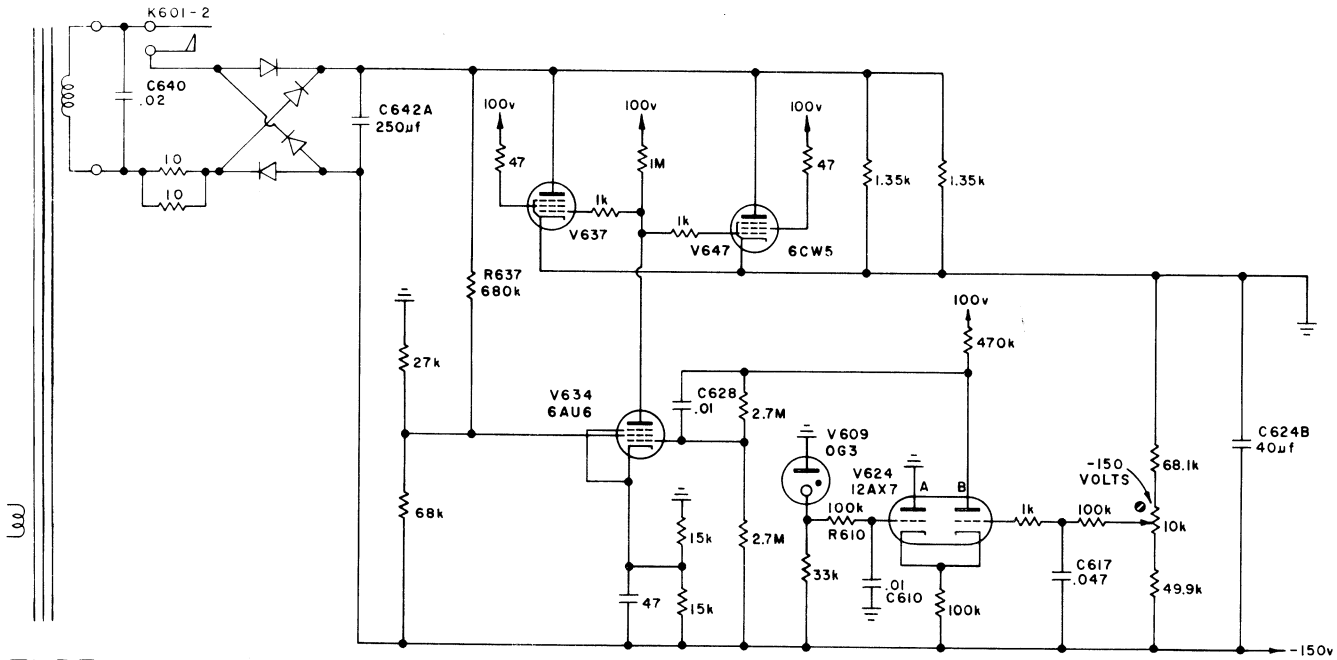
6. About 500 volts is supplied by the rectifier at 115v line.
   a. The unregulated bus will vary from 455v at 105v line to 555v at 125v line.
   b. C730 filters the rectifier output.
   c. R731 bleeds the capacitor charge.

7. Regulator operation is the same as the 100v regulator.
   a. A 6CW5 pentode (triode connected) is used as series regulator.
   b. The 40 ma requirement at low line is easily handled by the tube.

8. Since a regulated supply high enough to supply V724 plate is not available, the 350 unregulated is used.
   a. Ripple is introduced through R723 to V737 grid.
   b. This ripple is in phase with the ripple introduced through V737 plate.
   c. Ripple rejection, therefore, is rather poor.

J. -150v Supply

1. The -150v supply is a series regulated supply fed by a full wave silicon bridge.



TYPE 547 POWER SUPPLY
-150v SUPPLY

B-547-0076 x
5-13-'64 dl

2. The supply delivers an average of 300 ma.

   a. A connection to pin 9 of the blue ribbon connector (through a 100 decoupling resistor) supplies the plug-in -- the 1A1 uses 66 ma.

3. The supply uses a 206v transformer winding rated at .37 a.

4. A full wave silicon bridge supplies 275v DC to the regulator.
   a. The bottom of the supply is set at precisely -150v.
   b. The top of the supply ranges from 87v at 105v line to 135v at 125v line.
   c. The rectifier diodes are RCA 1N3194 750 ma silicon diodes with a 400v PIV.
   d. C640 reduces silicon switching transients.
   e. C642A filters the rectifier output.
5. An OG3 glow-dischrage voltage regulator tube is used as reference for the supply.
   a. 2 ma flows through the tube.
   b. It operates nominally at -84v.
   c. Voltage tolerance at 2 ma is 82v to 86v.
      (1) -150 VOLTS adjustment must be checked whenever the OG3 is changed.
6. The -150v supply has a 3 mv ripple spec (test spec) so like the 225v supply an additional gain stage is used.
7. The -150 VOLT adj, a screwdriver control, provides an adjustment whereby the -150v supply can be precisely adjusted.
   a. The -150v supply has a ±2% test spec so it is permissable to adjust the -150 VOLTS to bring one of the positive supplies into spec.
   b. The -150 VOLTS contol is part of the error sensing divider.

8. V624, a 12AX7 dual triode, is connected as a cathode coupled amplifier or comparator.

   a. The comparator compares the error voltage from the sensing resistors on grid B with the reference voltage from the OG3 on grid A.

   b. Since this is a negative supply, error voltages appear with opposite polarity from the positive supplies.

      (1) An increased load requirement makes the -150v output less negative.

      (2) Increased line voltage causes the -150v to go more negative.

   c. Unlike the 225v supply, the cathode coupled amplifier <u>does</u> invert the error signal.

      (1) The amplified error voltage is taken across a load resistor on the V624B plate instead of A plate.

   d. The cathode coupled stage has a gain of about 20.

   e. C617 conducts fast changes directly to V624B grid, bypassing the error sensing resistors.

   f. R618 increases the grid load resistance, providing a higher impedance for C617 to work into.

   g. R610 and C610 decouple glow tube noise from V624A grid.

   h. The comparator grids set at -84v.

   i. The cathodes set at -83v -- 830 μa flow through both cathodes.

   j. The plate sets at -5v.

9. The DC level at V624B plate is adjusted to -75.5v by a divider composed of R628, R629.
   a. The error signal is also attenuated by 50%.
   b. C628 couples fast changes around the divider.
10. V634 is the pentode error amplifier with a gain of about 150.
   a. The cathode sets at -74v.
   b. The screen is at -39v.
   c. The plate is pulled down to -5v at 115v line.
      (1) The plate potential ranges from -3v at 105v line to -6v at 125v line.
      (2) The plate has about 250 mv of ripple.
   d. Ripple is fed to the screen through R637 to aid in ripple rejection.
11. Two 6CW5 pentodes in parallel serve as series regulator CF's.
   a. 1k resistors in the grid circuit suppress parasitics.
   b. The tubes are pentode connected with the screens connected to the 100v regulated supply.
   c. The essentially flat pentode $e_p - i_p$ characteristics allow the tubes to operate over the 50v plate swing (from low line to high line) with little change in current.
   d. The pentodes high r_p makes tube current (and therefore cathode potential) virtually independent of the ripple on the plates.
12. C624B provides a low impedance to ground for transients too fast for the regulator to handle.
13. Dynamic output impedance is about .01Ω.

TYPE 547

XIV. CALIBRATOR

A. The calibrator supplies ≈1 KC square wave to the front panel jack (BNC).

1. 18 steps from .2 mv to 100v.
2. 100v DC.
3. 5 ma square wave through a current loop.
4. 5 ma DC through a current loop.

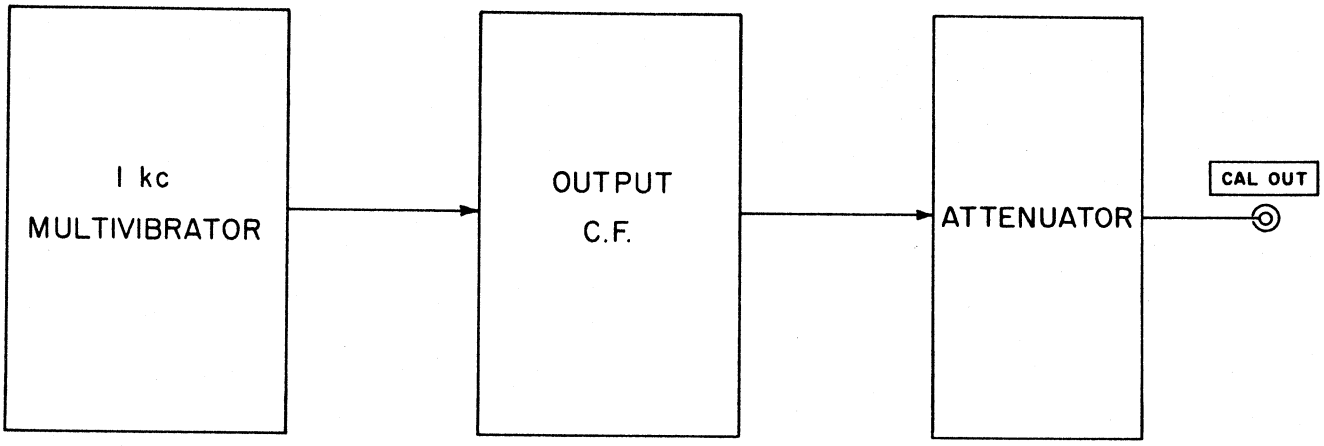
B. Operating Characteristics (Factory Spec)

1. Frequency approximately 1 KC (±25%).
2. Duty factor 45% to 55%.
3. Output voltage:
   a. .2 mv to 50v ±2%.
   b. 100v DC and 100v square wave ±1%.
   c. 4 ma ±2%.
4. Risetime:
   a. .2 mv to 4v, 300 nsec risetime (typically 180 nsec).
   b. 10v to 100v, 500 nsec (typically 350 nsec).

C. Output Impedance

1. 50 ohm in .2 mv to 200 mv positions.
   a. A 50 ohm load will reduce the amplitude by one-half.
2. Impedance increasing to 4k at 50v.
3. 420 ohms in 100v (AC and DC) positions.
4. Accuracy of 50 ohm impedance ±2%.

D. Block Diagram



TYPE 547 CALIBRATOR
BLOCK DIAGRAM

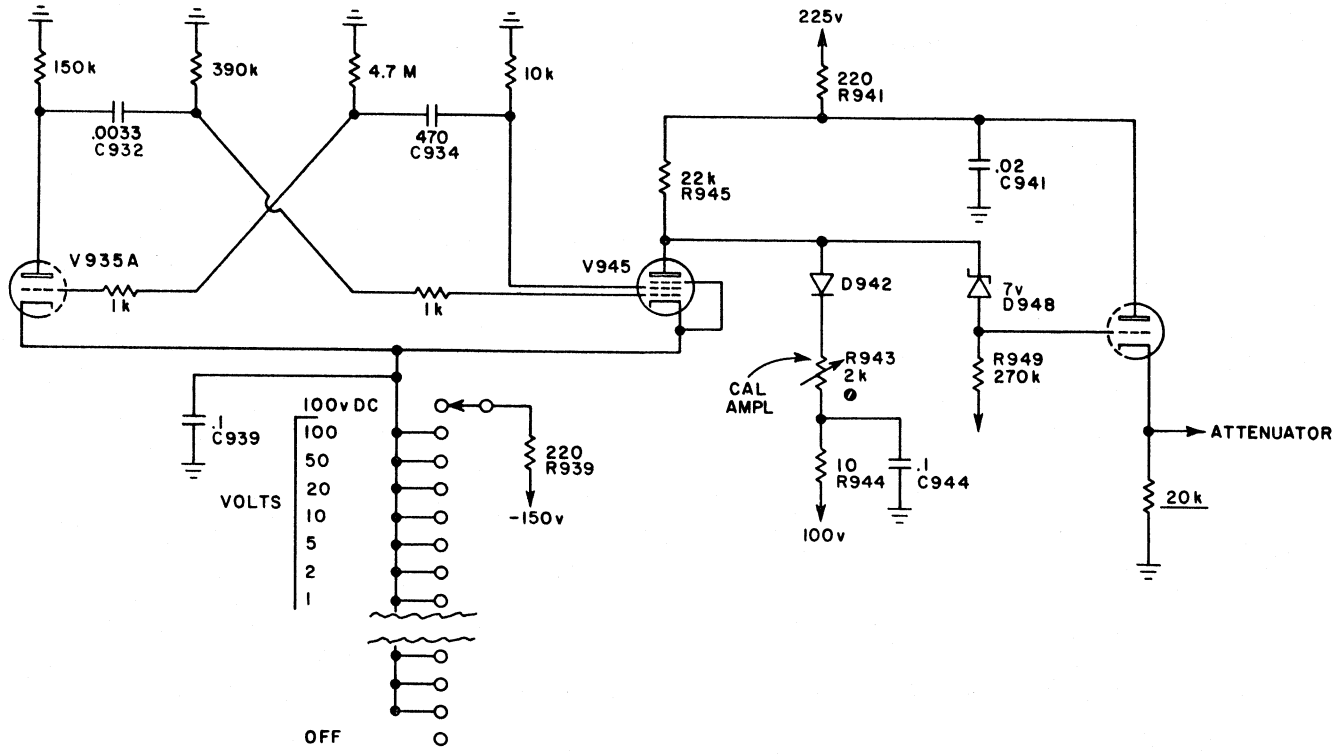
B-547-0062
4-15-'64 ms

E. Block Logic

1. The calibrator circuit consists of a 1 KC astable multivibrator driving an output CF.
2. The output is clamped at ground and 100v to provide a precise 100v peak-to-peak square wave.
3. A precision attenuator using 1% and 1/4% resistors attenuate the calibrator voltage for use at the CAL OUT jack.

F. Multivibrator

1. The multivibrator is a symmetrical, 1 KC plate coupled astable multi* using a half 12AU7 triode and a 6AU6 pentode.



TYPE 547 CALIBRATOR
MULTIVIBRATOR AND OUTPUT C.F.

B-547-0063x
4-17-'64 ms

2. The multi circuit differs from the basic multi design in that a triode and a pentode are used to achieve a relatively symmetrical output.

   a. The pentode screen serves as an anode and couples to the triode grid.

* See Typical Oscilloscope Circuitry, page 10-1.

b. The pentode plate operates as an electron-coupled amplifier.

(1) In this configuration, the pentode plates can rise rapidly while the screen is left to charge C934.

(2) The screen waveform has a risetime of 12 μsec, while the plate rises in about 180 nsec.

c. The pentode G_m (using the screen as an anode) is quite different from the triode.

(1) Plate load resistors, grid resistors and coupling capacitors are different to compensate for tube differences.

3. When the multi is turned on by the AMPLITUDE CALIBRATOR switch, the cathodes are tied to the -150v regulated supply.

4. The plate load resistors are connected to ground, effectively providing the multi with a 150v supply.

a. The grids have a positive return to ground, making multi switching less susceptible to noise than if they returned to the cathode potential.

5. When V945 conducts, its plate is pulled down to -55v.

a. There is about a 4v positive tilt to the bottom of the waveform.

b. The tilt (or exponential rise) is caused by a similar screen waveform.

c. The tilt to the screen waveform is caused by a relatively long time constant to the grid overshoot waveform -- about 500 μsec.

(1) When V935A cuts off, V945 grid is driven positive.

(2) The grid overshoot time constant = $(R931 + R_{g-k})$ C932 where R_{g-k} is the grid-to-cathode conduction resistances while grid current is flowing.

6. Risetime of the calibrator waveform is improved by tying V945 plate load resistor to 225v.

   a. When V945 cuts off, D942 catches the plate at 104v.

   b. The total plate rise (without diode limiting) is from -55v to +225v, but only the fast rise portion (0v to 104v) is used.

7. A zener, D948, provides a 7v offset from V945 plate to V933B grid.

   a. The 7v offset makes it possible to use the 100v regulated supply as reference for the 100v calibrator output.

   b. When V945 is cut off, a divider is formed between 222v (225v decoupled) and 100v, composed of R943, D942 and R945.

   c. When the CAL AMPL control is adjusted, V945 plate is caught at 104v.

   d. The 7v zener offset places the V935B grid at 97v.

   e. V935B works with 3v bias, placing the cathode at 100v.

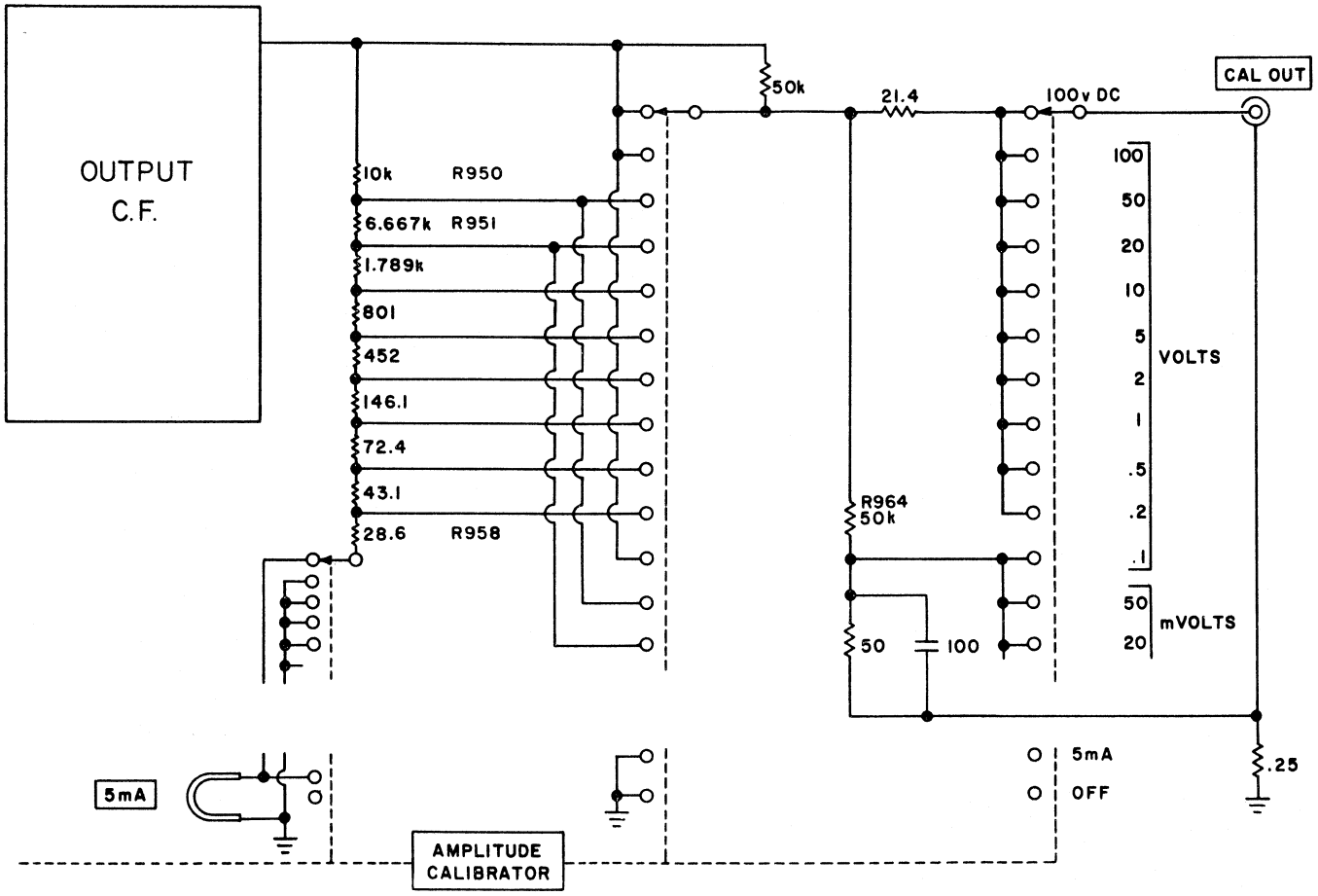
8. V935B cathode returns to ground through an equivalent 14.3k in the 100v position of the CAL switch.

   a. A total of 7 ma flows through the CF.

9. When V945 conducts and its plate pulls down to -55v, D942 uncouples and V935B cuts off.
   a. V935B cathode cannot go below ground so the waveform is limited at ground potential.
10. The output waveform, then, is shaped by being limited at the top by D942 and at the bottom by ground.
11. Decoupling keeps the fast switching transients out of the power supplies.
   a. R939, C939 decouples from the -150v supply.
   b. R941, C491 decouples from the 225v supply.
   c. R944, C944 decouples from the 100v supply.
12. R949 supplies zener keep-alive current.
13. R943, the CAL AMPL control (a screwdriver adjustment) allows precise adjustment of the 100v CAL output.
   a. It has a range of 8.8v.
   b. The control has adequate range if the 100v and 225v supplies and the diodes are within tolerance.

G. Attenuator

1. The attenuator divides the 100v square wave to the one current and 18 voltage positions.



TYPE 547 CALIBRATOR
ATTENUATOR

B-547-0064x
4-15-'64 ms

2. 100v DC position.

a. The cathode supply to the multivibrator is opened.

b. The output is clamped at 100v by D942 (set at 100v by the CAL AMPL control).

c. The 20k divider composed of R950 through R958 supplies 5 ma cathode current to V935B.

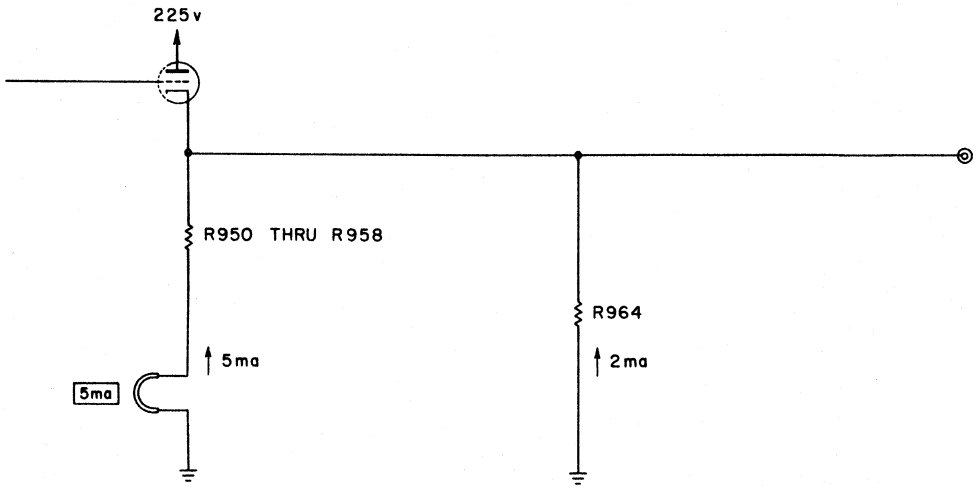
(1) The divider returns to ground through a front panel current loop to provide 5 ma DC.

3. 100v square wave position.

a. The 100v peak-to-peak square wave is connected directly to the CAL OUT jack.

b. R960 is shorted out.

4. In both 100v positions of the CAL switch, 5 ma flows through the divider and 2 ma flows through R964.



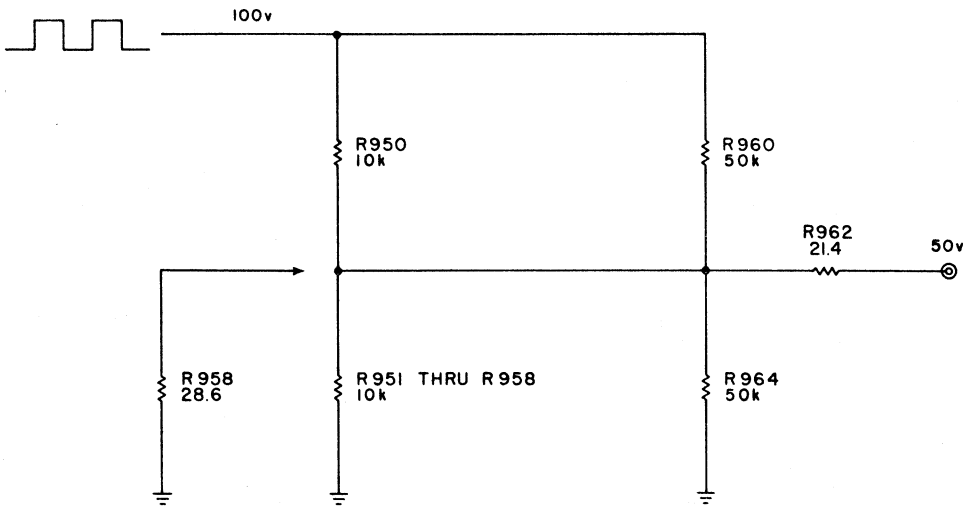
TYPE 547 CALIBRATOR
100v POSITIONS

B-547-0065
4-15-'64 ms

a. Output impedance is about 300 ohms.

(1) Cathode transimpedance shunted by 14k.

5. .2v to 50v positions.



TYPE 547 CALIBRATOR
50v POSITION

B-547-0066
4-15-'64 ms

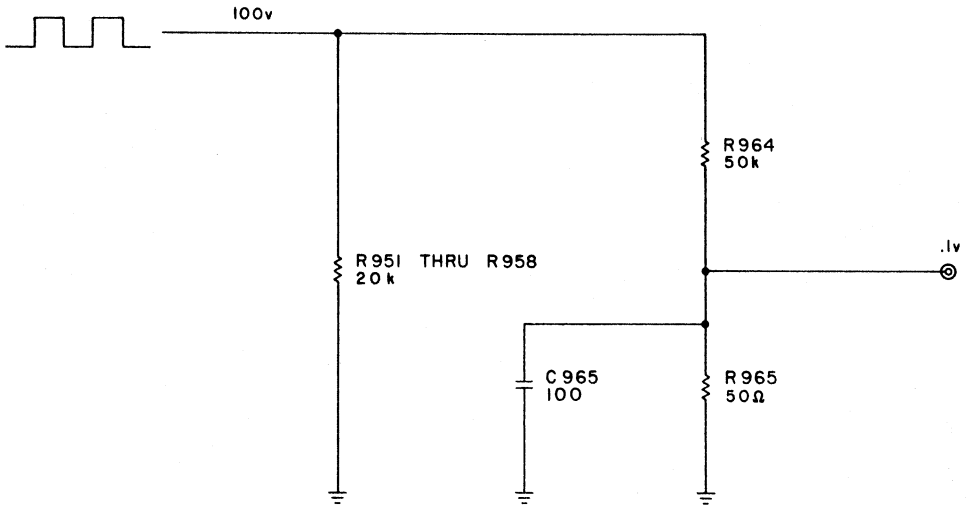
a. Taps on the divider R950 through R958 provide the voltage divisions.

b. In the .2v position, R962 adds to R958 to provide 50 ohm output impedance.

c. C958 (from R958 to ground) compensates the low impedance tap to prevent overshoot in the .2v position.

d. Impedance at switch positions .5v through 50v increase in impedance to about 4k at the 50v positions.

6. .1v position.



TYPE 547 CALIBRATOR
.1v POSITION

B-547-0067
4-16-'64 ms

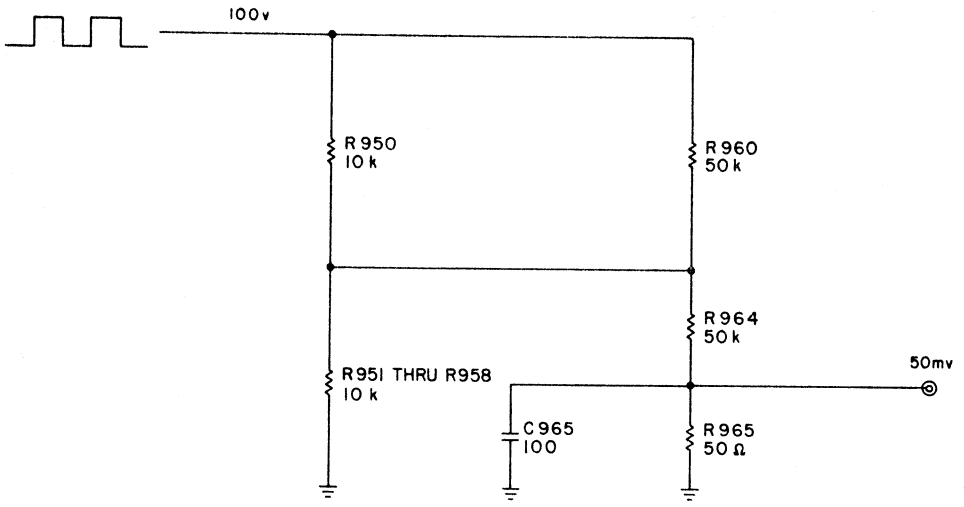
a. R960 is shorted out.

b. R964 and R965 form a 1000:1 divider.

c. R965 provides 50 ohm output impedance.

d. C965 compensates the low impedance portion of the divider to prevent overshoot.

7. .2 mv to 50 mv positions.



TYPE 547 CALIBRATOR
50mv POSITION

B-547-0068
4-16-'64 ms

a. These millivolt positions use the same taps on R951 through R958 as the corresponding voltage positions.

b. The square wave at volts amplitude is then divided to millivolts by R964 and R965.

c. Output impedance is 50 ohms.

d. C965 compensates the low end of the divider.

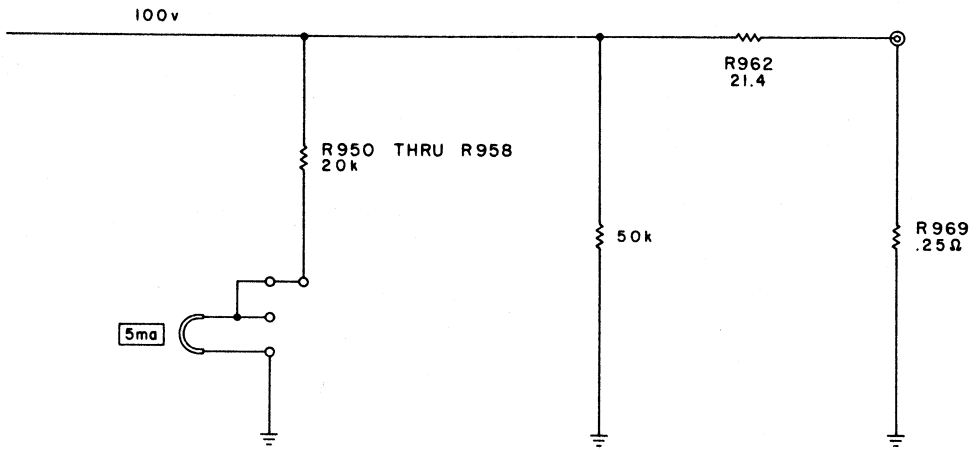
8. 5 ma⎍ position.

a. Current through the divider 20k string provides a 5 ma square wave through the current loop.

b. The current loop is provided primarily to calibrate a current probe.

c. The CAL OUT is disconnected in this position preventing accidental loading of the current square wave.

9. R969 placed between the CAL OUT jack ground return and grounc breaks up ground loops in the system when a coax is used at the CAL OUT jack.



TYPE 547 CALIBRATOR
GROUND LOOP RESISTOR

B-547-0069
4-15-'64 ms

547 SLIDES

1. Vertical Amplifier

B-547- 0037
0038
0039
0040
0041
0042
0043
0044

2. Sweep Generators

B-547- 0010
0011
0011.1
0092
0012
0092.1
0013
0092.2
0092.3
0014
0015
0016
0092.4
0017
0018
0019
0020
0021
0093

3. Horizontal Display Modes

B-547- 0082
0077
0078
0094
0079
0094.1
0030
0079
0077
0080
0081

4. Horizontal Amplifier

B-547- 0056
0057
0058
0059
0060
0061

5. Alternate Sweep Switching

B-547- 0022
0023
0024
0025
0084
0026
0085
0027
0086
0028
0030
0087
0029
0088
0031
0032
0089

6. Trigger Circuits

B-547- 0045
0046
0047
0048
D-12a-0003
B-547-0049

7. Delay Pick-Off

B-547- 0033
0034
0035
0036

8. Multi-Trace Sync Amp

B-547- 0083
0090
0090.1
0090.2
0091
0091.1
0091.2

9. CRT Circuit

B-547- 0050
0051
0052
0053
0054
0055

547 Slides (cont.)

10. Low Voltage Power Supply

B-547- 0070
0071
0072
0073
0074
0075
0076

11. Calibrator

B-547- 0062
0063
0064
0065
0066
0067
0068
0069

Appendix 2

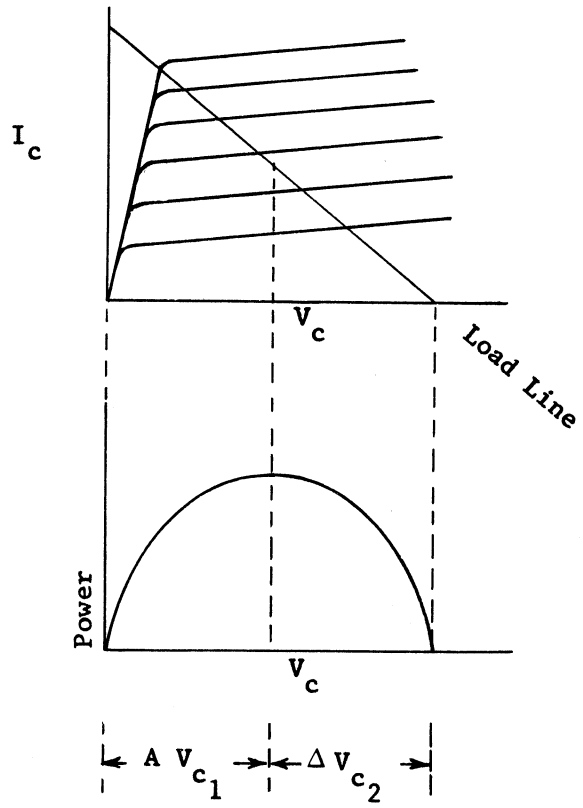
TEMPERATURE COMPENSATION IN PUSH-PULL TRANSISTOR AMPLIFIERS

The gain of a transistor depends (among other things) on the β and the r_e (emitter dynamic resistance) of the transistor. At a fixed I they both tend to increase with temperature. Temperature is a direct function of power dissipation in the transistor.

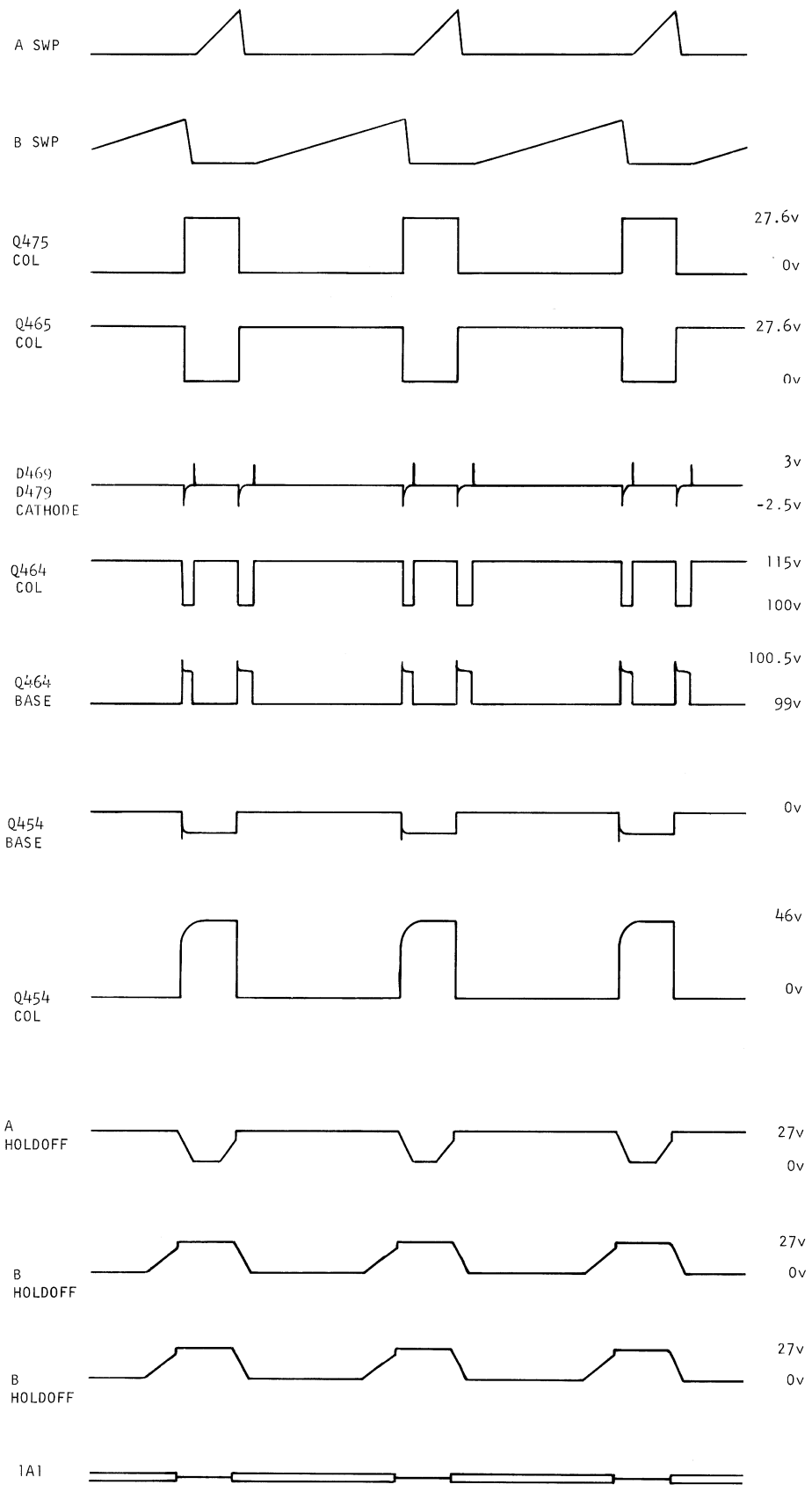
In the design of a push-pull amplifier, the selection of collector loads to assure matched power dissipation is an important consideration.

Collector loads may be chosen so the transistor operates quiescently on the maximum power dissipation point on the load line. From this point (as suggested by the curve at the right), either higher or lower values of V_c will reduce power dissipation.

If a DC signal voltage is applied to a push-pull amplifier, collector voltage will increase in one transistor and decrease in the other. If the collector loads have been properly selected, power dissipation will fall off equally in both transistors. If power dissipation remains balanced, transistor temperatures remain balanced.



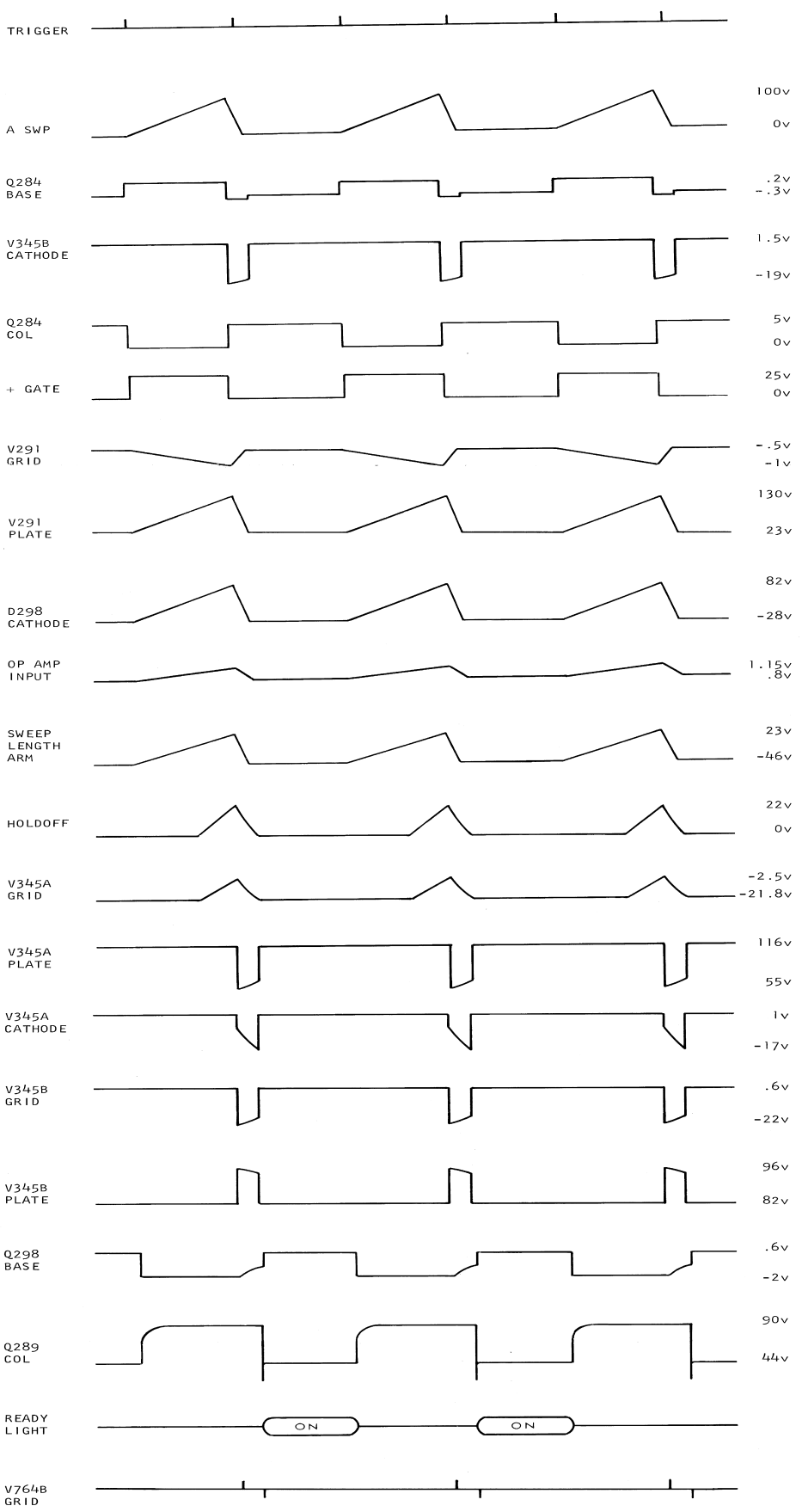
SCOPE UNDER TEST	FREE RUN
MODE: A ALT. B	
A SWEEP: 10 μ sec/cm	
B SWEEP: 20 μ sec/cm	
TEST SCOPE: .1 msec/cm	



WAVEFORMS A ALT B FREE RUN

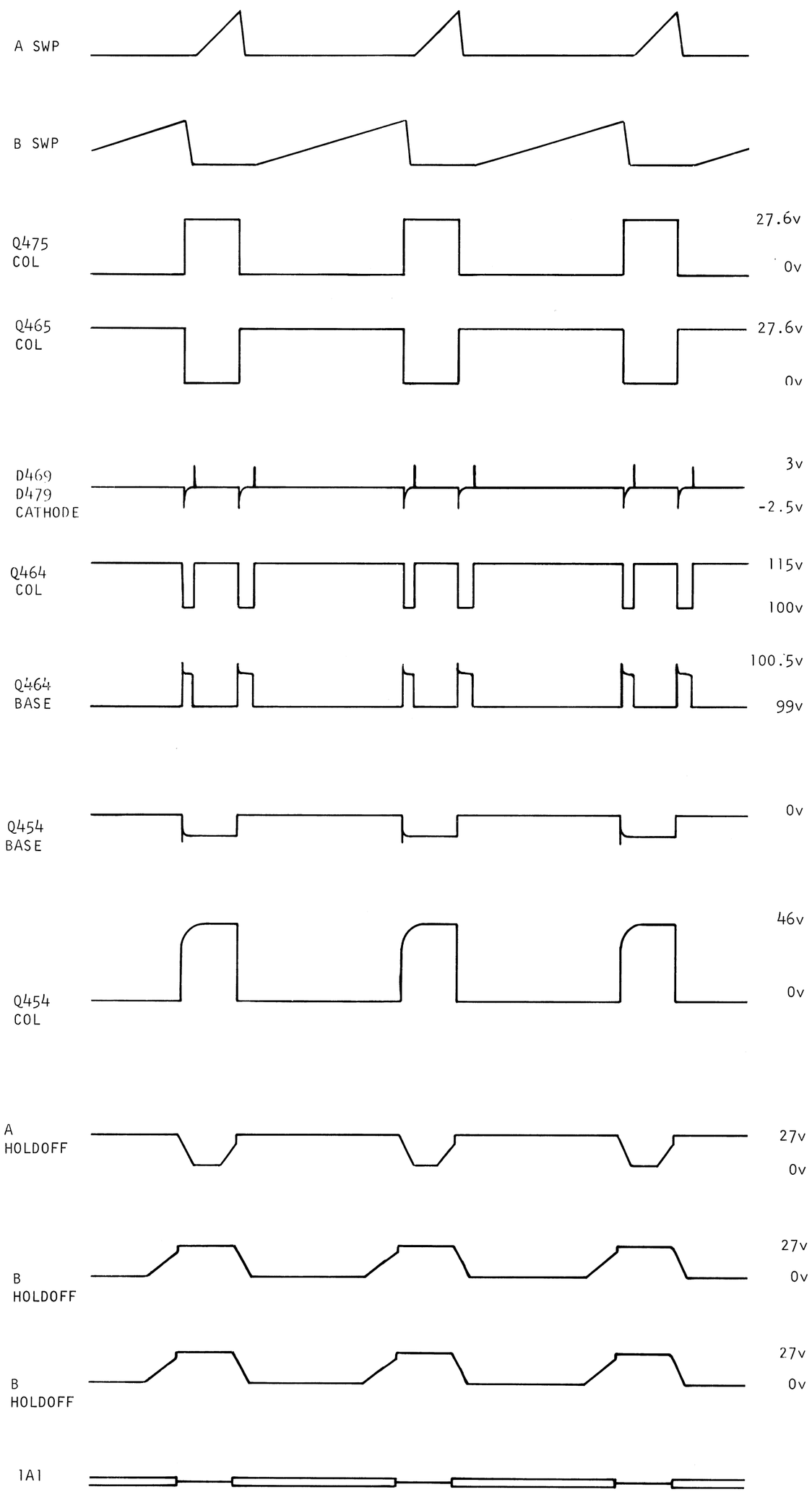
SCOPE UNDER TEST
TRIGGERED BY CAL
MODE: A ONLY
SWEEP: .1 msec/cm

TEST SCOPE: .5 msec/cm

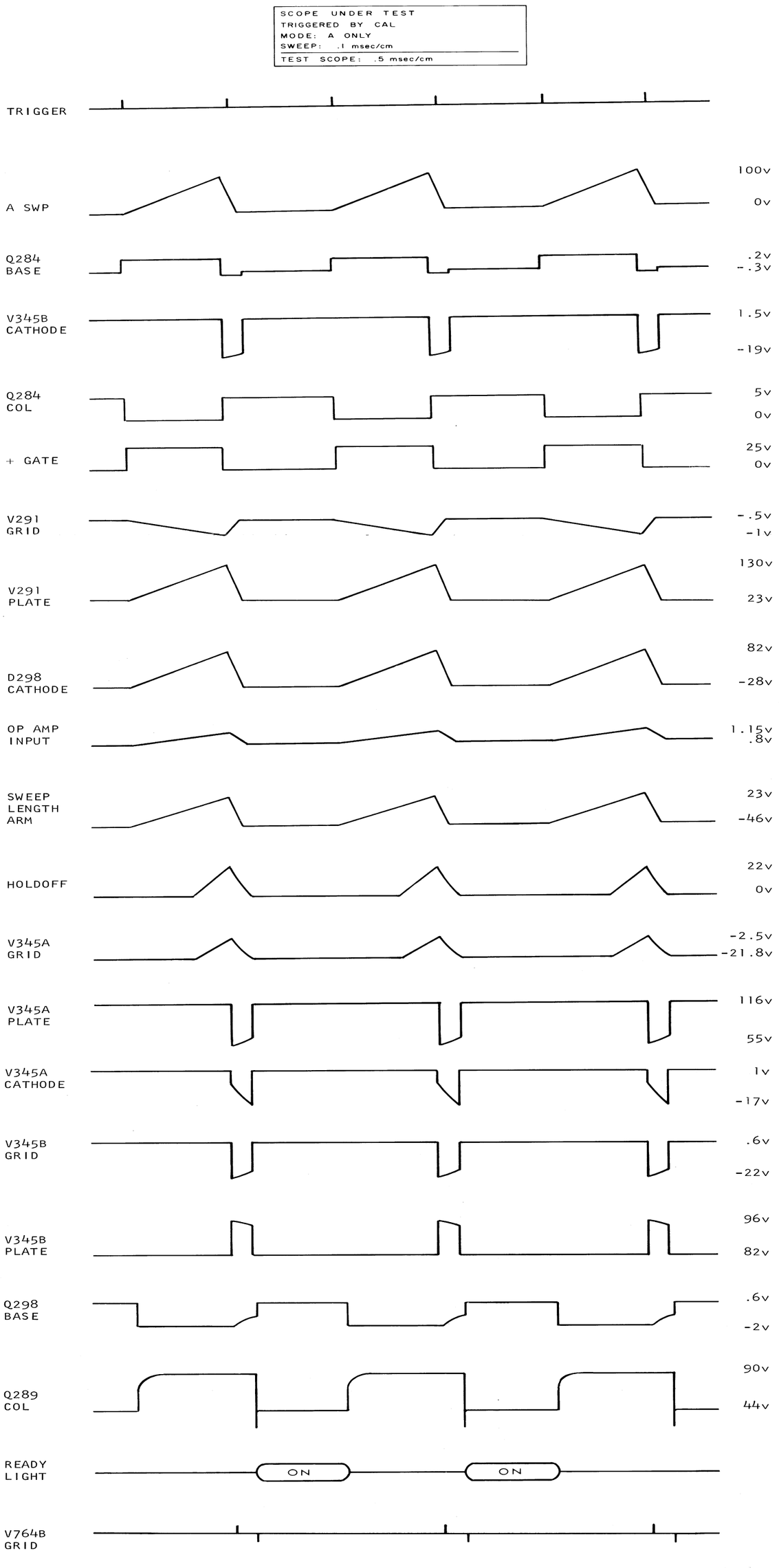


WAVEFORMS A SWEEP

SCOPE UNDER TEST	FREE RUN
MODE: A ALT. B	
A SWEEP: 10 μ sec/cm	
B SWEEP: 20 μ sec/cm	
TEST SCOPE: .1 msec/cm	



WAVEFORMS A ALT B FREE RUN



WAVEFORMS A SWEEP